

PROJECT NAME : BAL22 15" , BAL32 17"
PCB NO : LA-D803P(Bristol)

Dell / Compal Confidential

Schematic Document

AMD Bristol

AMD R16M-M70 (23 X 23mm) +GDDR5 x4

2016-06.21 Rev: 1.0 (A00)

@ : Un-pop Component

FX_R3@/A12_R3@/A10_R3@:APU R3 PN

FX_R1@/A12_R1@/A10_R1@:APU R1 PN

45@/ HDMI LOGO

PCB@/ MB part number

PCB_R3G@/PCB_R3T@PCB_R3H@:PCB R3 PN

ST@ / stoney only

BR@ /Bristol only

4G_S@/4G_M@/4G_H@/2G_H@/2G_M@/2G_S:VRAM Strap Pin:

S4G_R1@:samsung R1/ H4G_R1@:Hynix R1 /M4G_R1@ :Micron R1

S4G_R3@:samsung R3/ H4G_R3@:Hynix R3 /M4G_R3@ :Micron R3

DIS@/ GPU only

M30@/ R16M1-M30

M70@/R16M1-M70

M30_R3@/M70_R3@:GPU R3 PN

M30_R1@/M70_R1@:GPU R1 PN

UMA@/ UMA only

TI@/PARADE@/NRDSA@ : SATA

3234@/3246@ :Audio

EMI@/ESD@/RF@ : EMI, ESD ,RF Component

@EMI@/@ESD@/@RF@ : EMI, ESD,RF unpop

KBBL@:for KB backlight use

PTP@/NPTP@/TP_WAKE@:Touch pad

HDT@ /Debug use

| | | | | | | |
|---|--------------------|-----------------|------------|--------------------------|------------------------|---------------|
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| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | Cover Page | |
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VRAM 256M*16
GDDR5 *4
Page 38,39

64bit

AMD R16M-M1-70
FCBGA631
35W 23x23mm
Page 33-40

PEG 2.0 x4

eDP Conn.
Page 16

DP0

eDP

HDMI Conn.
Page 17

DPI

DDI

AMD
Bristol
Processor
BGA 968

PCI-E

Port 1
x1
NGFF 2230
WiFi/BT4.0
Page 20

Port 0
x1
Ethernet
RTL8106E
10/100
Page 19

SATA HDD Conn.
Page 22

Port 0
SATA Rediver
Page 22

SATA3.0

SATA ODD Conn.
Page 22

Port 1
SATA3.0

SPI ROM
128MB
Page 10

SPI

LPC Bus
33MHz

ENE KBC
KB9022QD
Page 27

I2C

PS/2

Int.KBD
with KBBL
Page 24

Touch Pad
Page 24

FAN CONN
Page 24

Thermal Sensor

Memory Bus Bristol support two CHs

DDR4-DIMM X2
1.2V DDR4
Page 13-14

USB 3.0

Port 1

USB 3.0 Conn. 1
USB 2.0 Conn. 1
Page 23

Port 2

USB 3.0 Conn. 2
USB 2.0 Conn. 2
Page 23

USB2.0

Port 2

Port 6
USB 2.0 Conn. 3
For DB

Port 4
NGFF 2230
WiFi/BT4.0
Page 20

Port 7
Digital Camera /IR Camera
(With Digital MIC)
Page 16

Port 5
Touch Screen
Page 16

Port 0
Card Reader
RTS5170
Page 21

Port 2

Digital Mic.

HD Audio

Audio Codec
ALC3234
Page 18

Headphone Jack /
Mic. Jack combo
On IO/B
Page 25

Int. Speaker R / L
Page 18

SUB-BOARDS

ODD BOARD

I/O BOARD

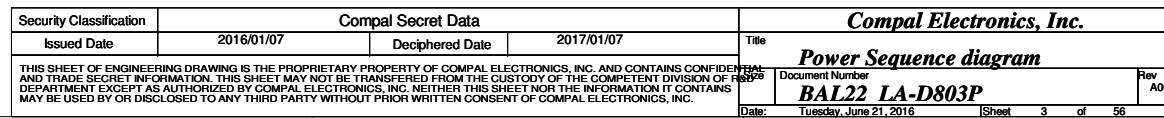
I/O BOARD

POWER BOARD

LED BOARD

| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|------------------------------|
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2016/04/13



Board ID Table for AD channel

| | | | | | |
|----------|-------------|-------------|-------------|-------------|-------------|
| Vcc | 3.3V +/- 1% | | | | |
| Ra | 100K +/- 1% | | | | |
| Board ID | Rb | VAD_BID min | VAD_BID typ | VAD_BID max | EC AD3 |
| 0 | 0 | 0.000V | 0.000V | 0.300V | 0x00 - 0x13 |
| 1 | 12K +/- 1% | 0.347V | 0.354V | 0.360V | 0x14 - 0x1E |
| 2 | 15K +/- 1% | 0.423V | 0.430V | 0.438V | 0x1F - 0x25 |
| 3 | 20K +/- 1% | 0.541V | 0.550V | 0.559V | 0x26 - 0x30 |
| 4 | 27K +/- 1% | 0.691V | 0.702V | 0.713V | 0x31 - 0x3A |
| 5 | 33K +/- 1% | 0.807V | 0.819V | 0.831V | 0x3B - 0x45 |
| 6 | 43K +/- 1% | 0.978V | 0.992V | 1.006V | 0x46 - 0x54 |
| 7 | 56K +/- 1% | 1.169V | 1.185V | 1.200V | 0x55 - 0x64 |
| 8 | 75K +/- 1% | 1.398V | 1.414V | 1.430V | 0x65 - 0x76 |
| 9 | 100K +/- 1% | 1.634V | 1.650V | 1.667V | 0x77 - 0x87 |
| 10 | 130K +/- 1% | 1.849V | 1.865V | 1.881V | 0x88 - 0x96 |
| 11 | 160K +/- 1% | 2.015V | 2.031V | 2.046V | 0x97 - 0xA4 |
| 12 | 200K +/- 1% | 2.185V | 2.200V | 2.215V | 0xA5 - 0xAF |
| 13 | 240K +/- 1% | 2.316V | 2.329V | 2.343V | 0xB0 - 0xB7 |
| 14 | 270K +/- 1% | 2.395V | 2.408V | 2.421V | 0xB8 - 0xBF |
| 15 | 330K +/- 1% | 2.521V | 2.533V | 2.544V | 0xC0 - 0xC9 |
| 16 | 430K +/- 1% | 2.667V | 2.677V | 2.687V | 0xCA - 0xD4 |
| 17 | 560K +/- 1% | 2.791V | 2.800V | 2.808V | 0xD5 - 0xDD |
| 18 | 750K +/- 1% | 2.905V | 2.912V | 2.919V | 0xDE - 0xF0 |
| 19 | NC | 3.000V | 3.300V | 3.300V | 0xF1 - 0xFF |

BOARD ID Table

| Board ID | |
|----------|--------------|
| 0 | bristol EVT |
| 1 | bristol DVT1 |
| 2 | bristol DVT2 |
| 3 | bristol XB |
| 4 | |
| 5 | |
| 6 | |
| 7 | |
| 8 | |
| 9 | |
| 10 | Stoney |
| 11 | Stoney |
| 12 | Stoney |
| 13 | Stoney |
| 14 | Stoney |
| 15 | Stoney |
| 16 | Stoney |
| 17 | Stoney |
| 18 | Stoney |
| 19 | Stoney |

SMBUS Control Table

| | SOURCE | BATT | Charger | | DIMM | | Thermal Sensor | |
|------------------------------|---------|------|---------|--|------|--|----------------|--|
| EC_SMB_CK1 EC_SMB_DA1 | KB9022Q | V | V | | | | | |
| EC_SMB_CK2 EC_SMB_DA2 | KB9022Q | | | | | | V | |
| EC_I2C_TPCLK EC_I2C_TPDAT | KB9022Q | | | | | | | |
| APU_SCLK0 APU_SDATA0 | APU | | | | V | | | |
| APU_SCLK1 APU_SDATA1 | APU | | | | | | | |
| APU_SIC APU_SID | APU | | | | | | V | |

Symbol Note :

 : means Digital Ground

 : means Analog Ground

CLOCK SIGNAL

| | |
|--------------|------------------|
| CLKOUT_PCIE0 | 10/100 LAN |
| CLKOUT_PCIE1 | NGFF Card (WLAN) |
| CLKOUT_PCIE2 | |
| CLKOUT_PCIE3 | |
| | |
| GFX CLK | dGPU |

ULT

USB3.0

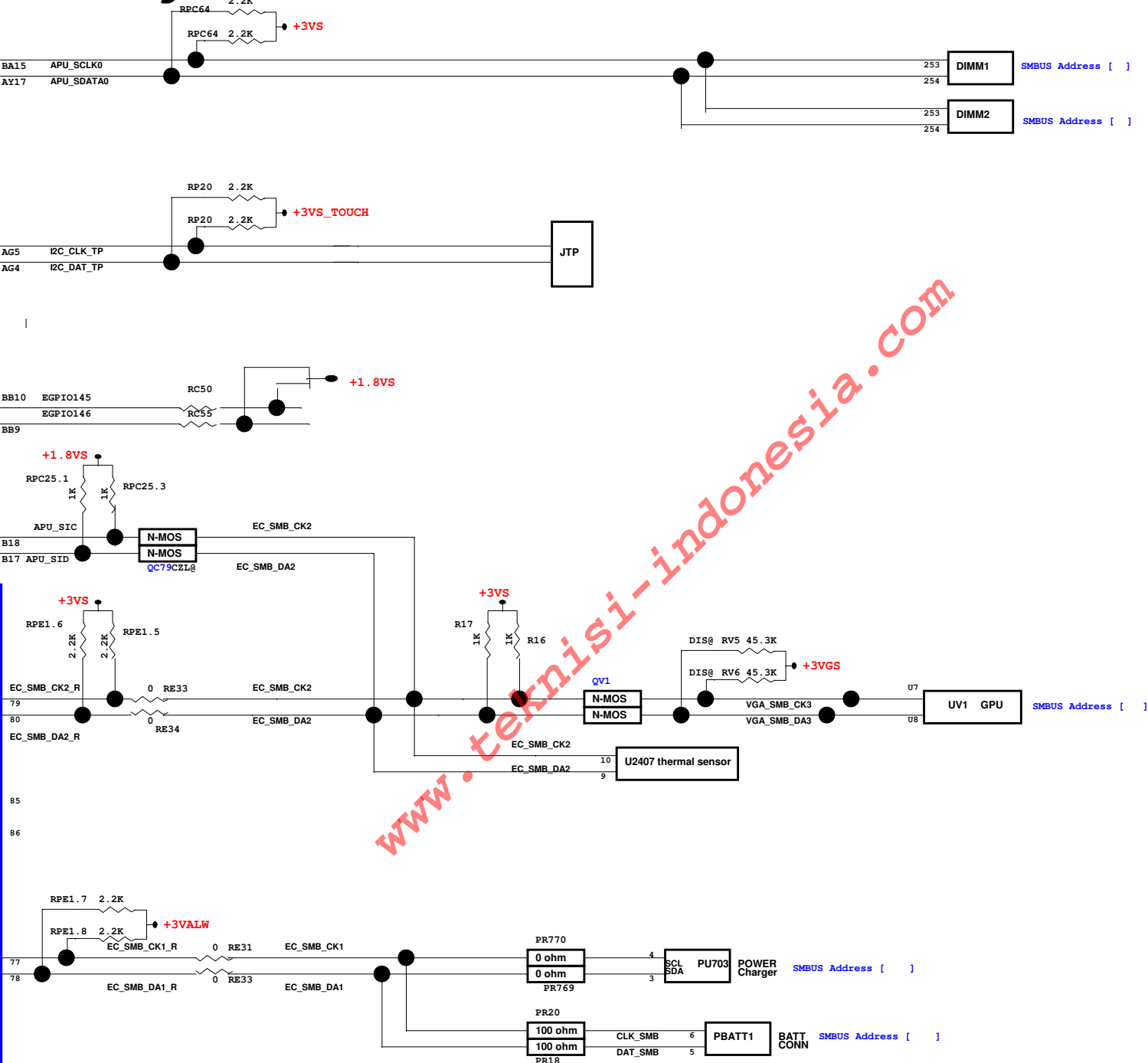
| | |
|-------------|----------------------|
| Port1 | NA |
| Port2 | USB3 connector 1 |
| Port3 | USB3 connector 2 |
| Port4 | NA |
| USB2.0 | |
| Port0 | Card Reader |
| Port1 | Touch Screen Panel |
| Port2 | Camera |
| Port3 | USB connector 1(D/B) |
| Port4 | NGFF Card (WLAN) |
| Port5 | USB connector 1 |
| Port6 | USB connector 2 |
| Port7 | NA |
| PCI EXPRESS | |
| Lane 1 | 10/100 LAN |
| Lane 2 | NGFF Card (WLAN) |
| Lane 3 | |
| Lane 4 | |
| Lane 5 | PEG (AMD)M70 |
| Lane 6 | PEG (AMD)M70 |
| Lane 7 | PEG (AMD)M70 |
| Lane 8 | PEG (AMD)M70 |
| SATA | |
| SATA0 | HDD |
| SATA1 | ODD |

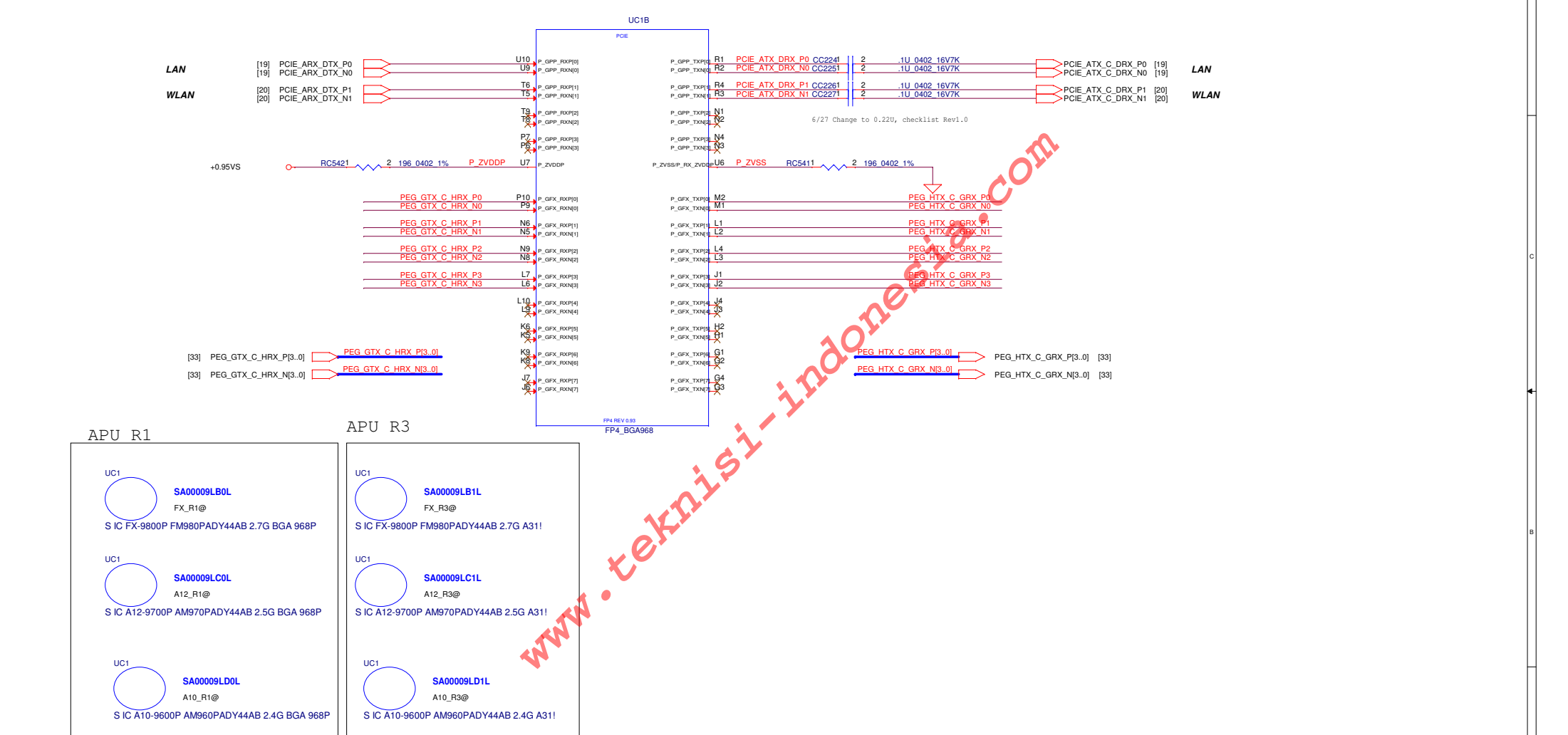
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SMBus Block Diagram

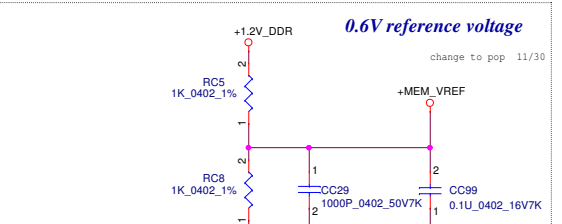
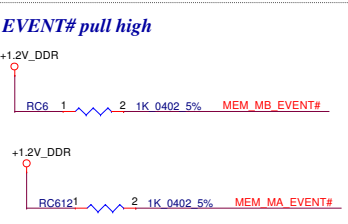
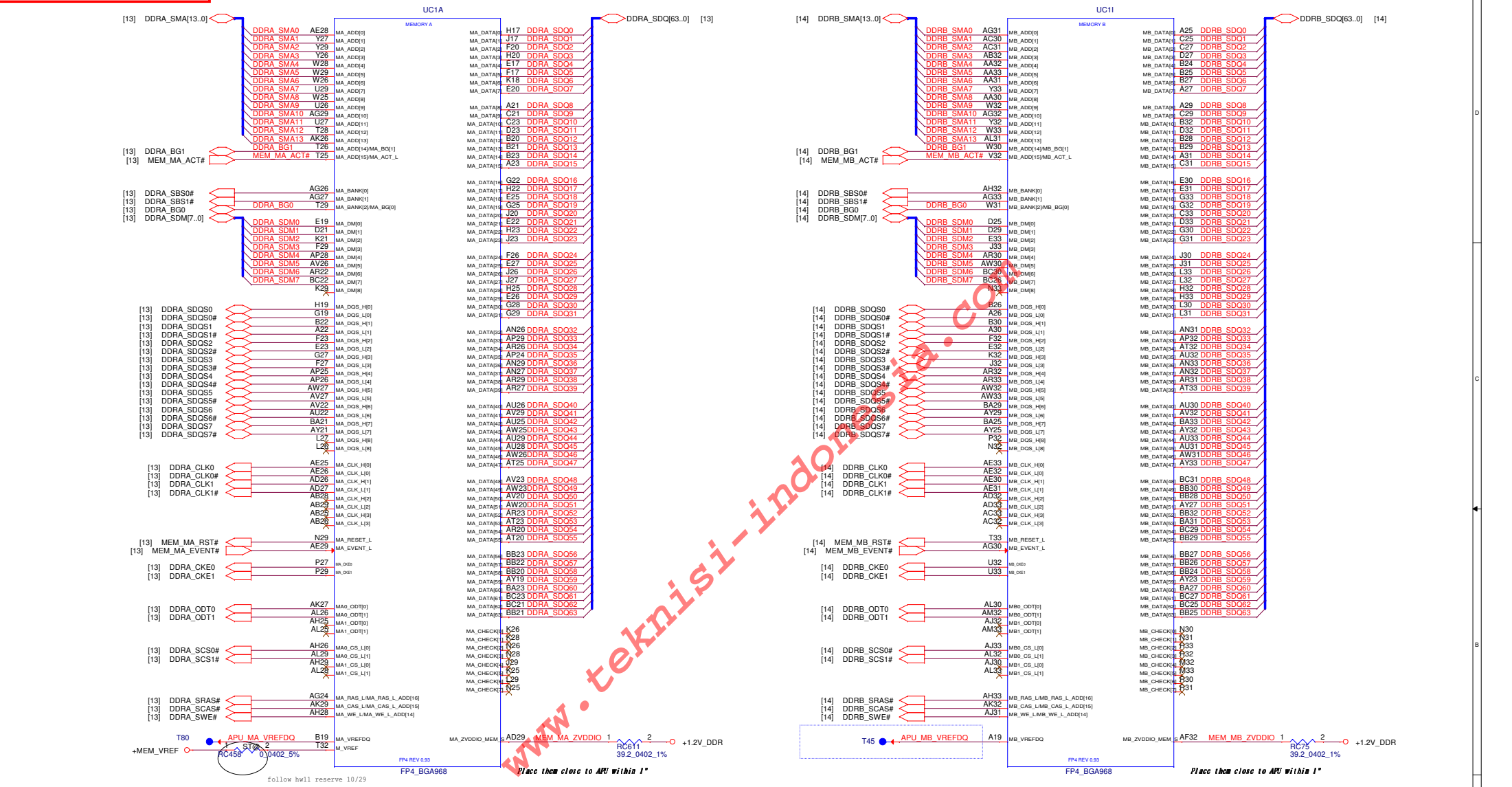
Bristol

KBC
KB9022QD



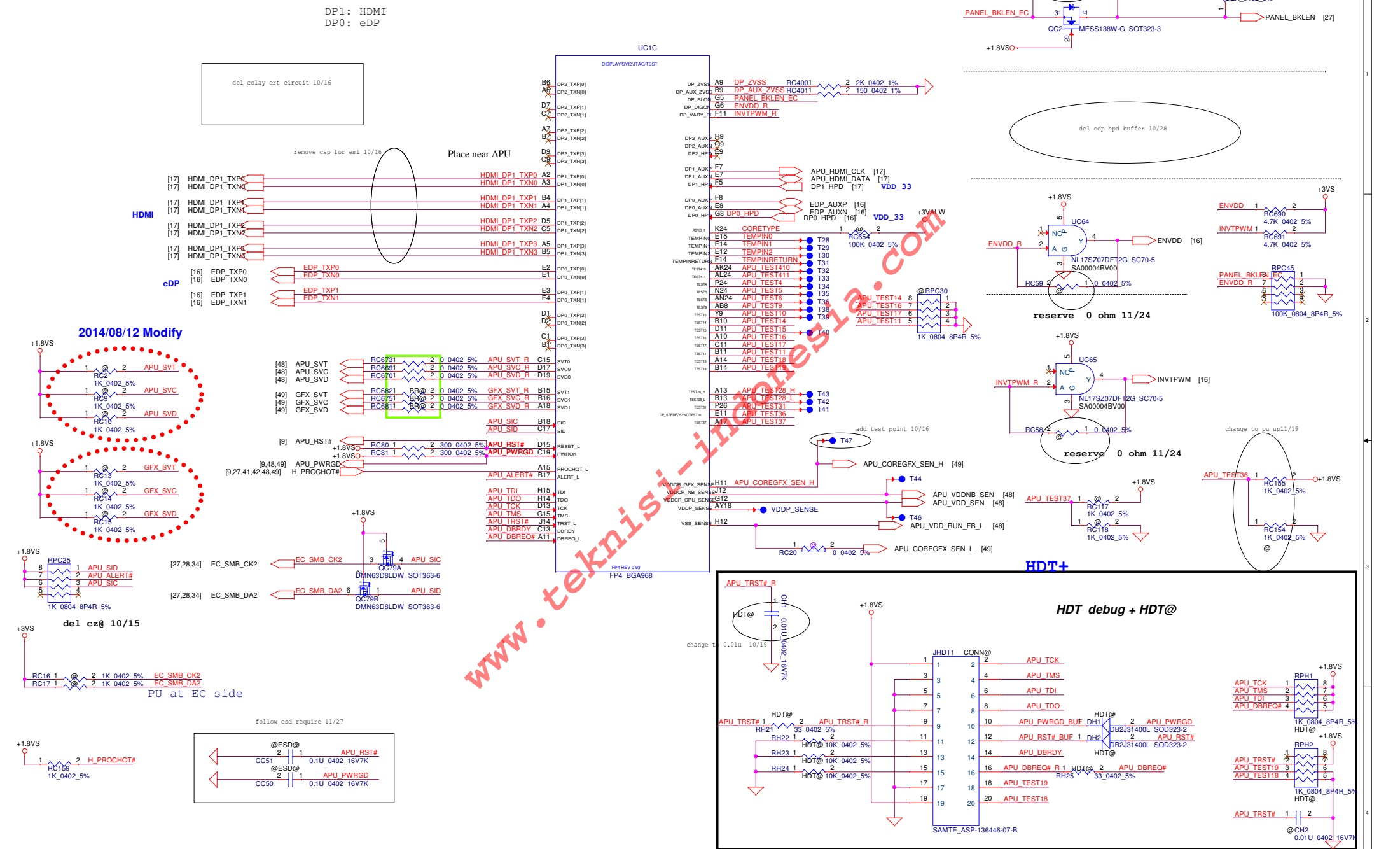


Main Func = CPU



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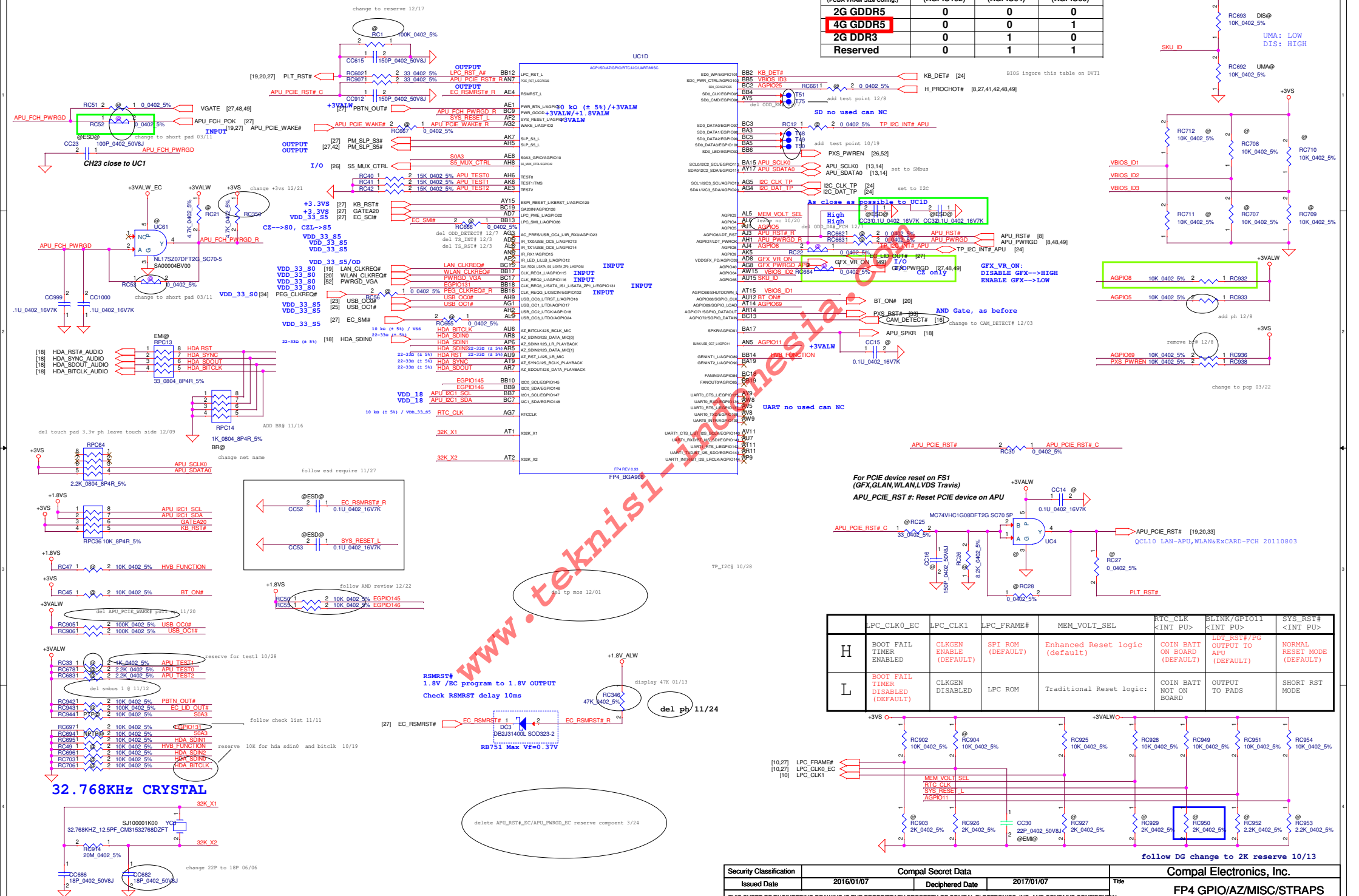
Main Func = CPU



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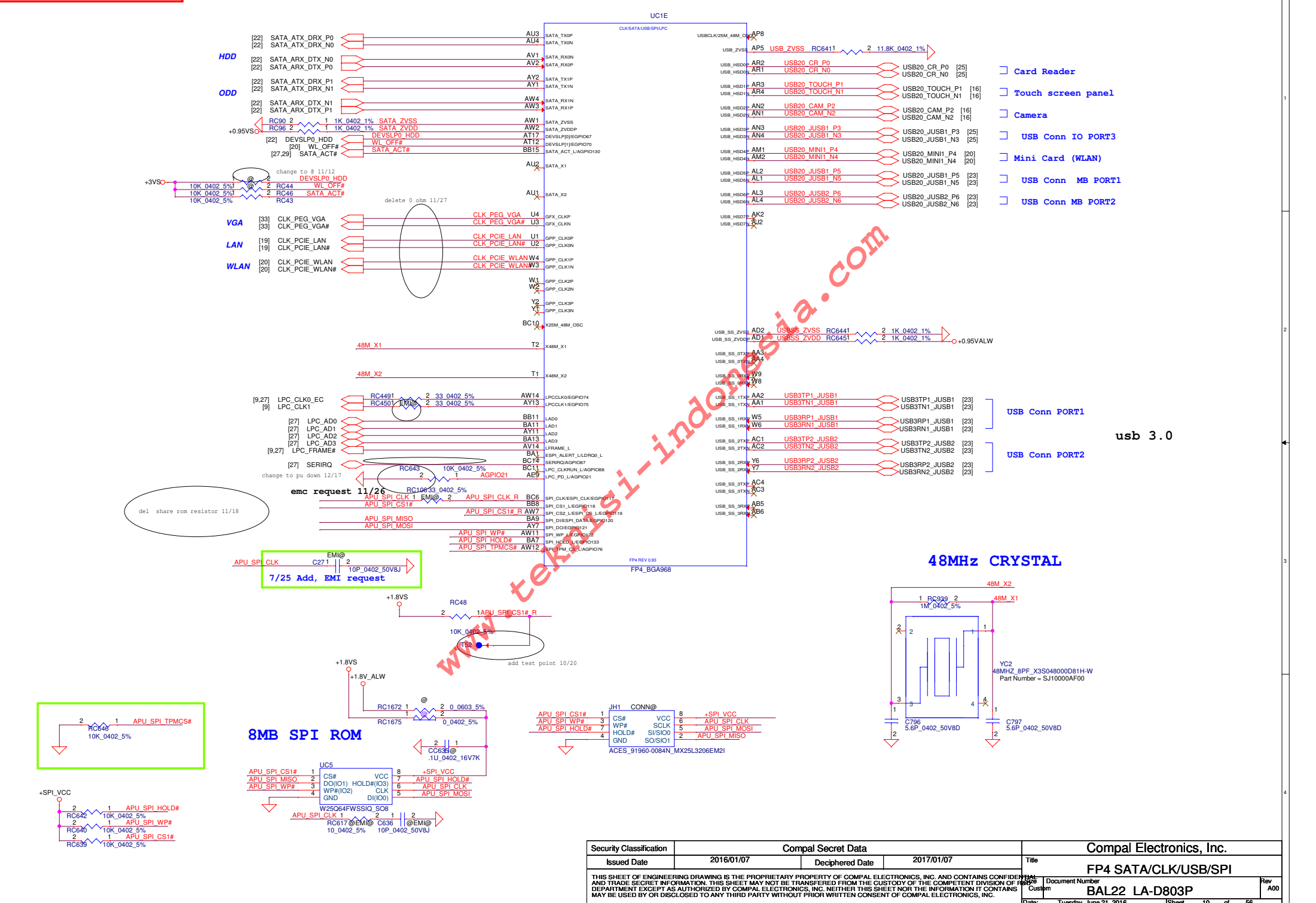
Main Func = CPU

| VBIOS (PCBA VRAM Size Config.) | VBIOS_ID3 (AGPIO102) | VBIOS_ID2 (AGPIO64) | VBIOS_ID1 (AGPIO66) |
|--|--------------------------------|-------------------------------|-------------------------------|
| 2G GDDR5 | 0 | 0 | 0 |
| 4G GDDR5 | 0 | 0 | 1 |
| 2G DDR3 | 0 | 1 | 0 |
| Reserved | 0 | 1 | 1 |



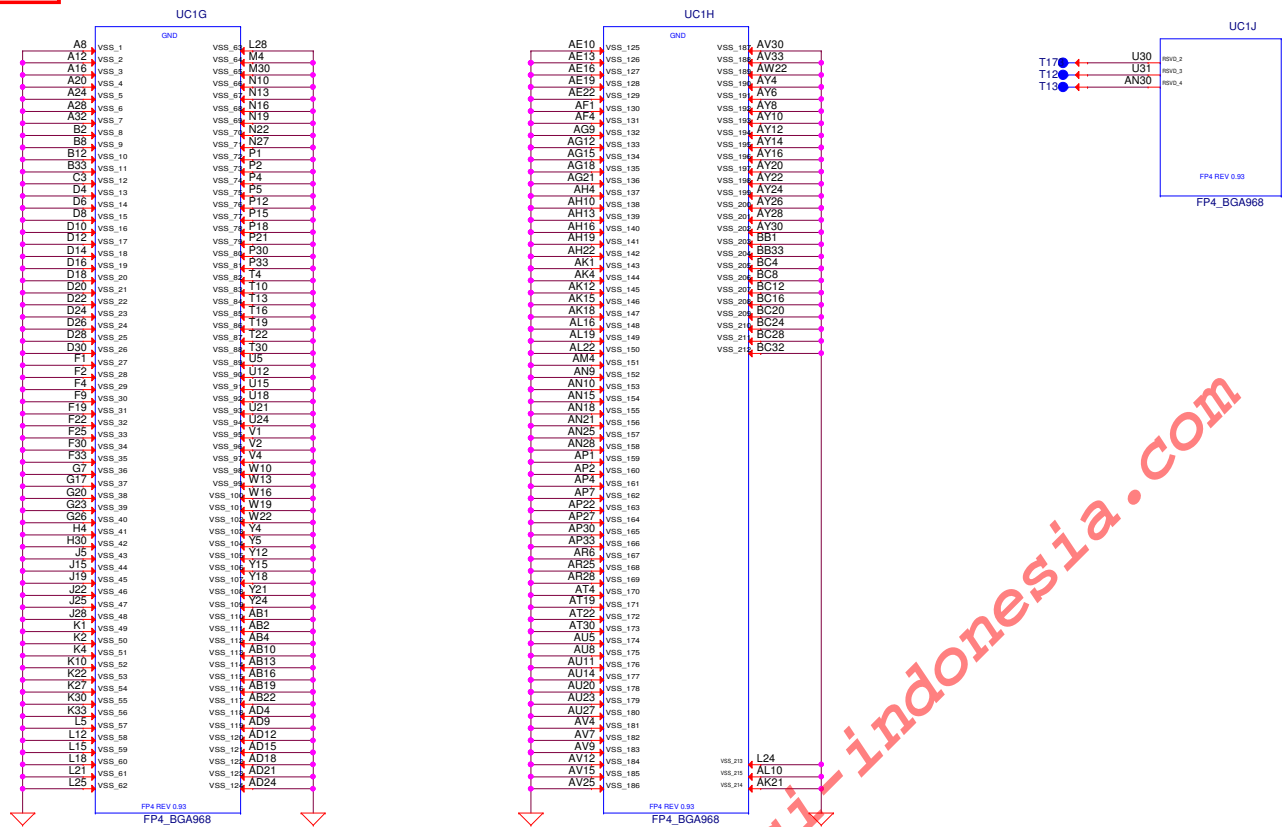
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Main Func = CPU

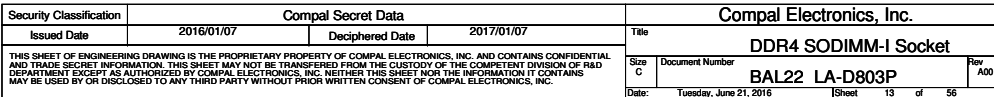


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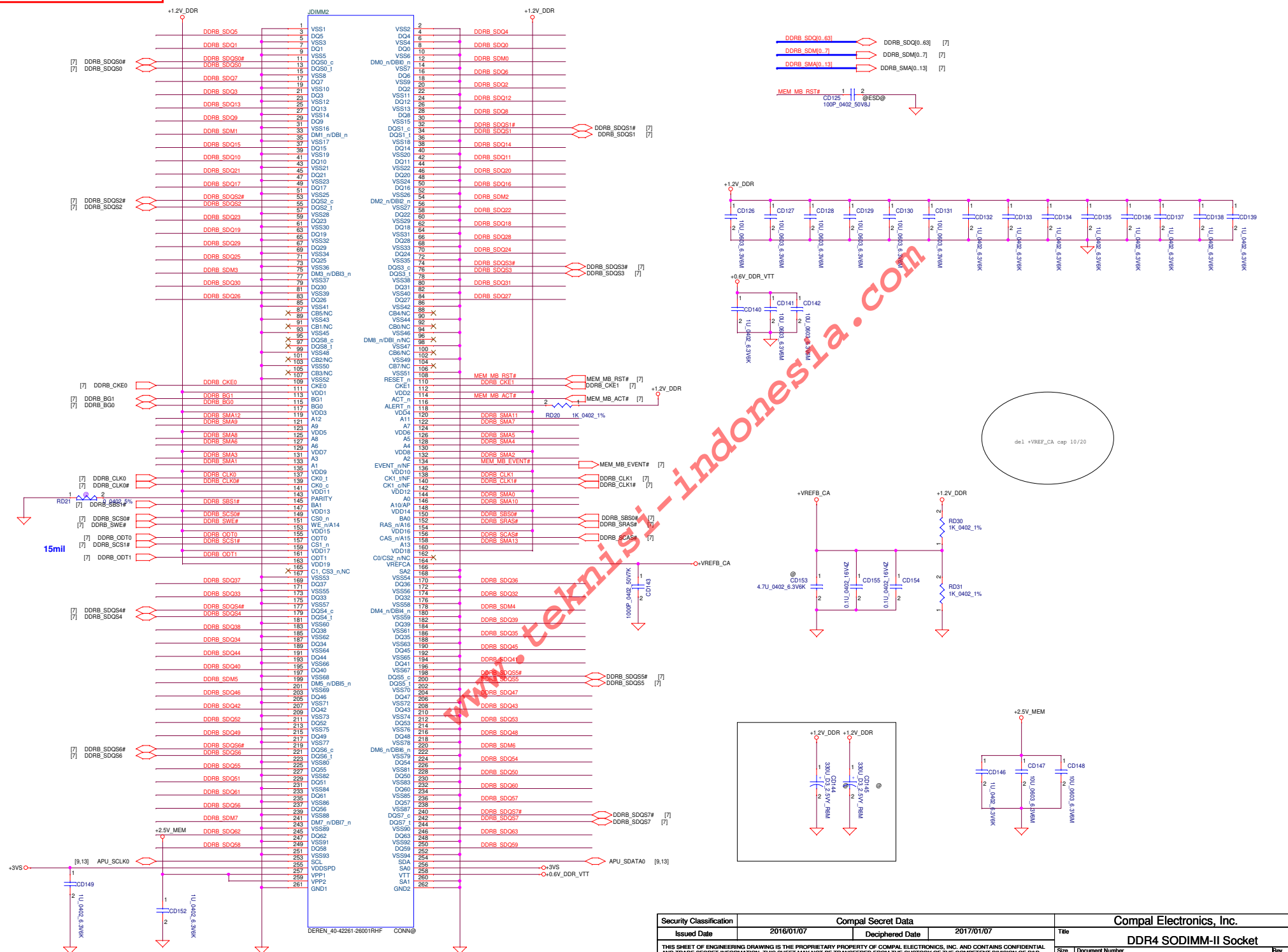
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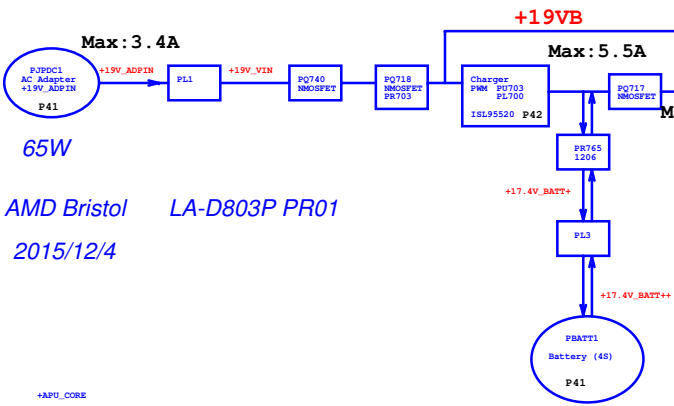
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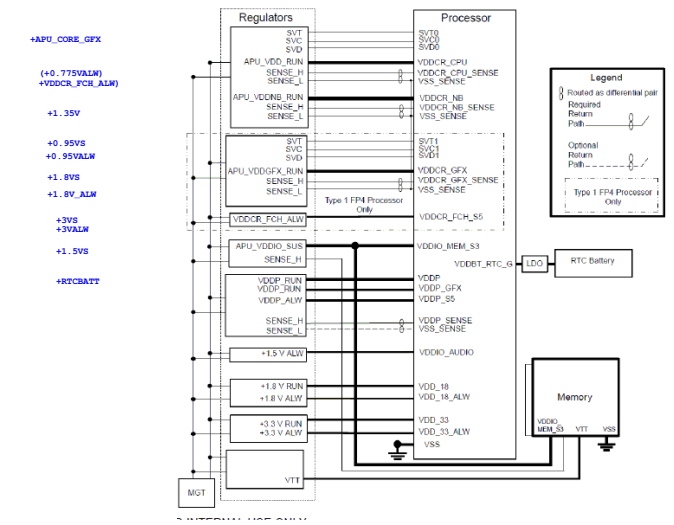
Main Func = DIMM2



| | | | | | |
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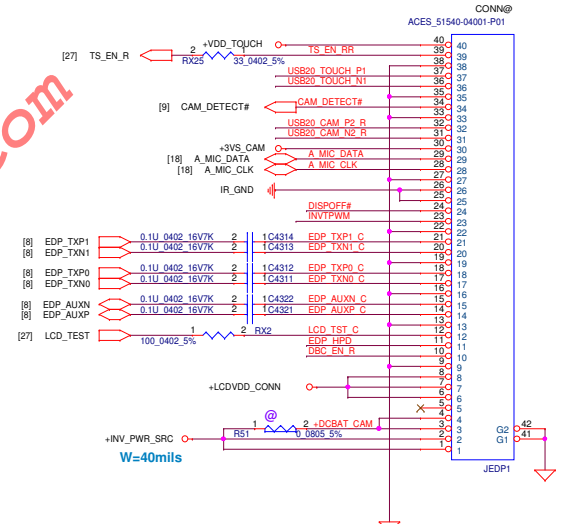
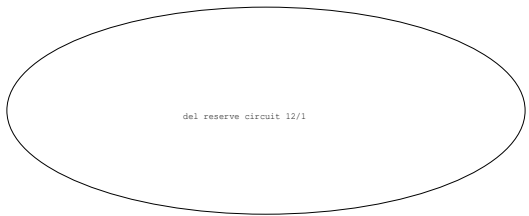
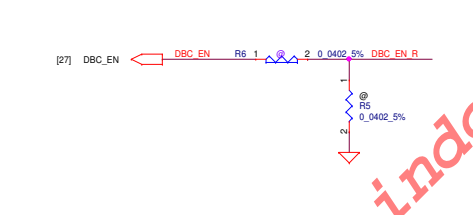
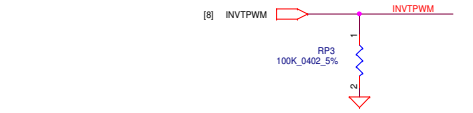
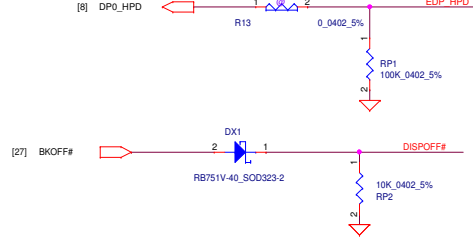
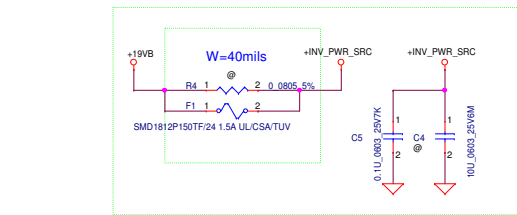
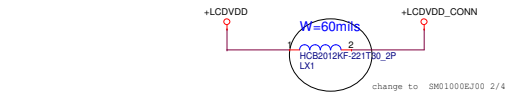
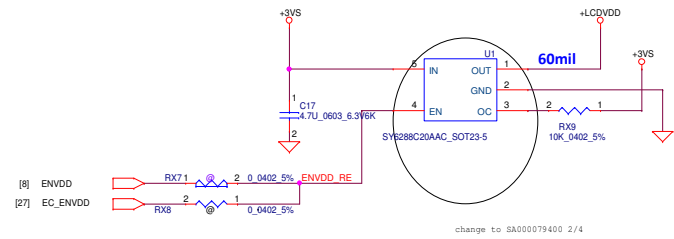
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2015/12/4



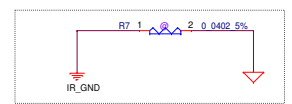
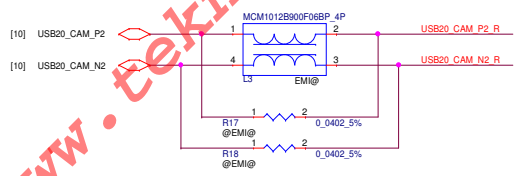
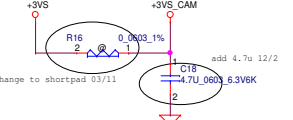
| FP4 Supply Name | Purpose | Nominal voltage |
|-----------------|---------------------------------|----------------------------------|
| VDDCR_CPU | CPU Cores | Variable |
| VDDCR_NB | Northbridge, etc. | Variable |
| VDDCR_GFX | Graphics Cores | Variable |
| VDDCR_FCH_S5 | FCH & USB | Variable |
| VDDIO_MEM_S3 | MEM PHY | DDR3 = 1.5V, 1.35V, DDR4 = 1.20V |
| VDDP | PCIE & DISPLAY PHYs | |
| VDDP_GFX | x8 dGPU PCIE PHY | 1.05V |
| VDDP_S5 | USB PHYs | |
| VDD_18 | PLLs | 1.8V |
| VDD18_S5 | RTC, USB2, USB3 | 1.8V |
| VDD_33 | GPIO (S0), SDIO, I2C, LPC, etc. | 3.3V |
| VDD_33_S5 | GPIO (S5), USB2 | 3.3V |
| VDDIO_AUDIO | AZ, I2S | 1.5V (AZ)/1.8V (I2S) |
| VDDBT_RTC_G | RTC | 1.5V |

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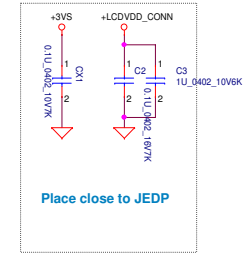
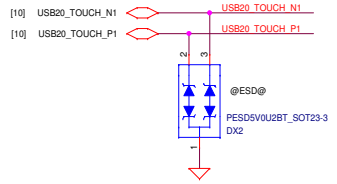
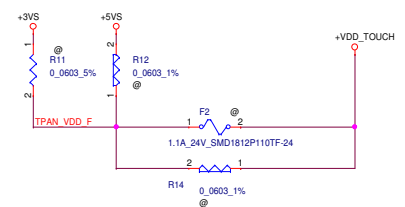
Main Func = LCD



Webcam PWR CTRL

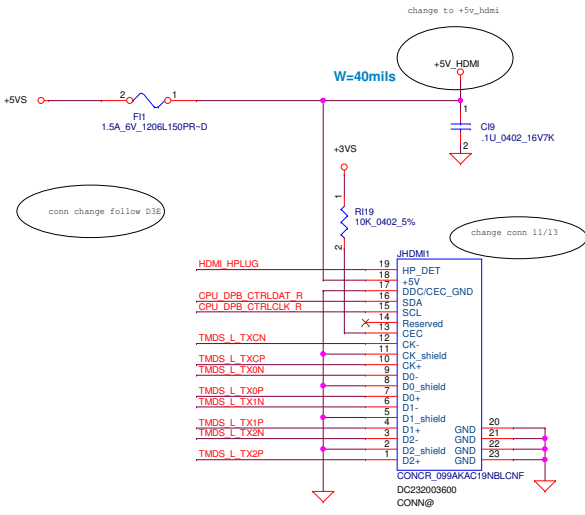
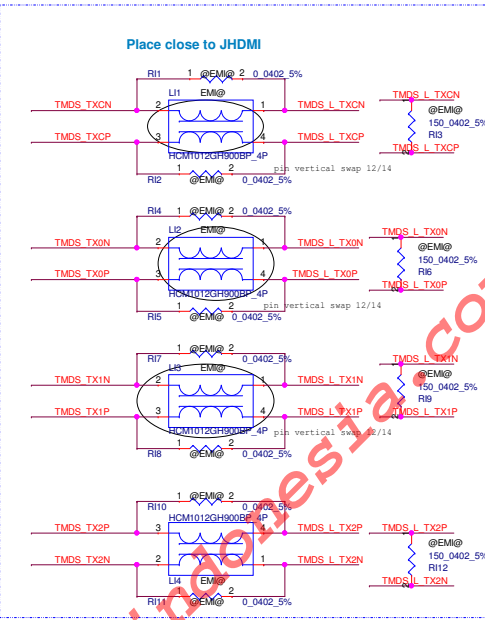
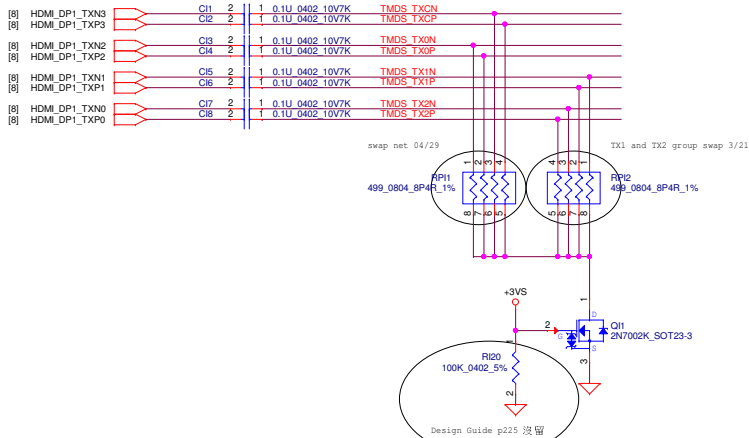


* Touch Screen Panel



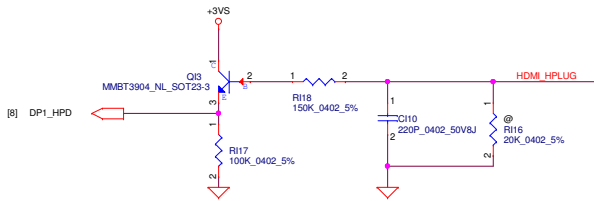
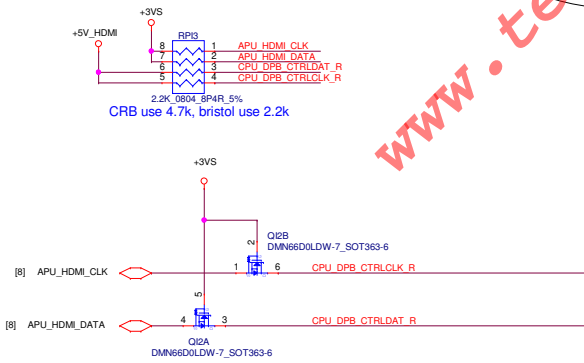
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| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | eDP / webcam / TouchScreen |
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| | | | | | BAL22 LA-D803P |
| | | | | Date: | Tuesday, June 21, 2016 |
| | | | | Sheet | 16 of 56 |

Main Func = HDMI

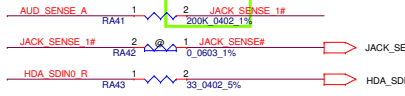
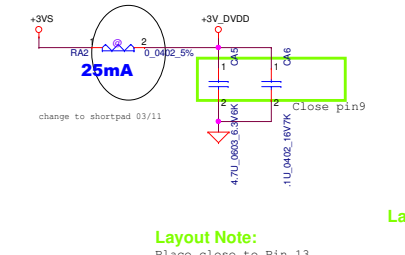
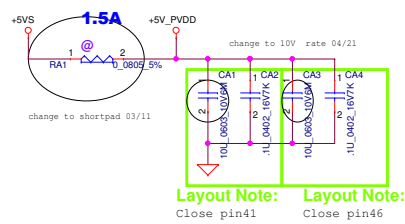


Main: LTCX0064K00 (CIS ok)
(TEMP:DC021407310)

| Part Number | Description |
|---------------------|-------------|
| ROYALTY HDMI W/LOGO | |



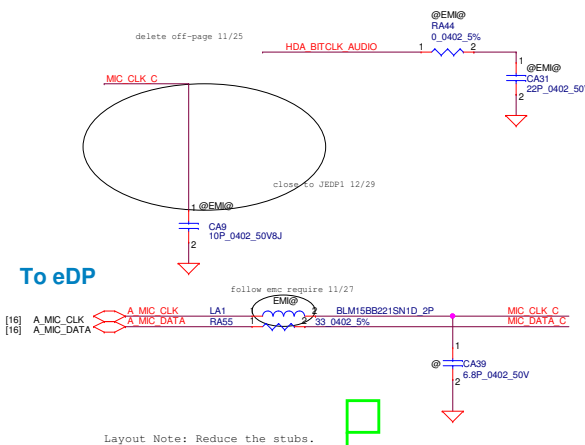
Main Func = Audio



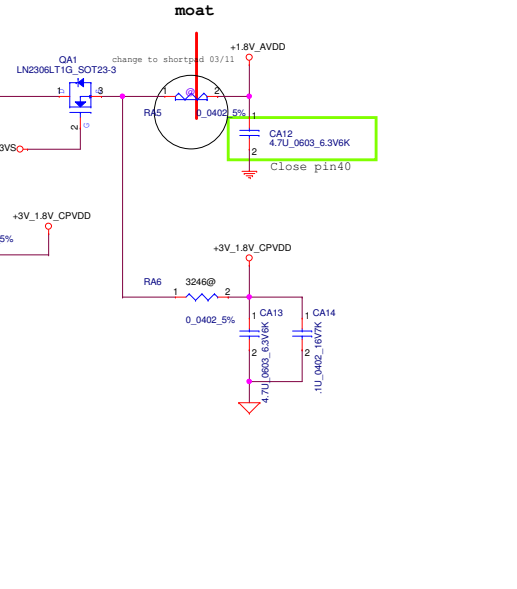
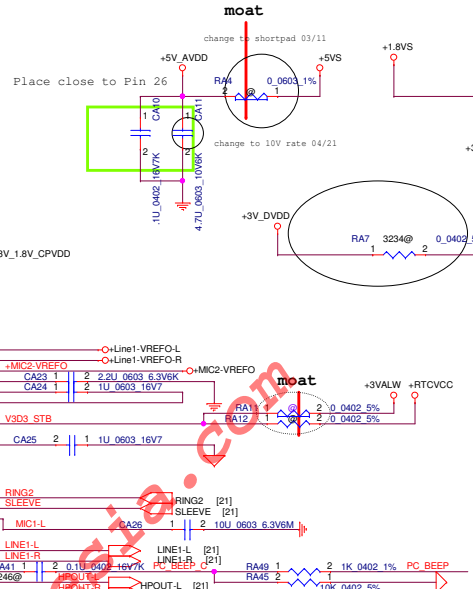
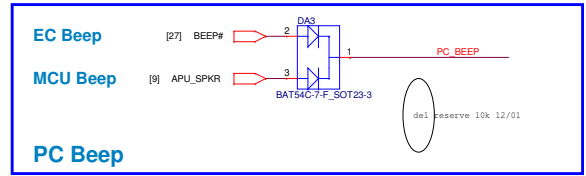
C6230, C6231 close to UA1 pin1

Layout Note: Speaker trace width >40mil @ 2W4ohm speaker power

Layout Note: Place close to Pin 13



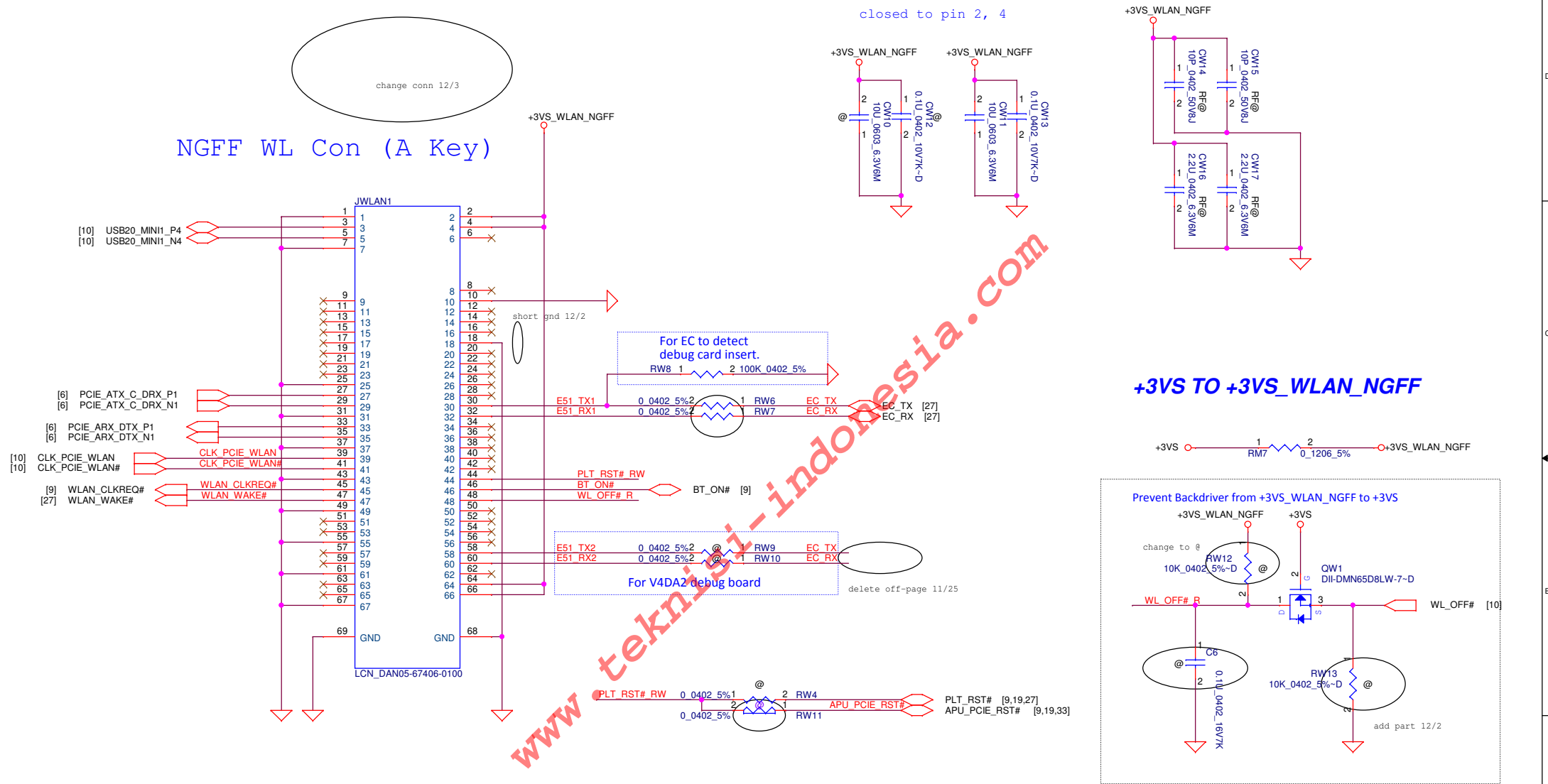
Trace width for SPK-L-/SPK-L-/SPK-R-/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil



| | | | | | |
|--|--|------------------------|--|---------------------|--|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | | Deciphered Date | | Document Number | |
| 2016/01/07 | | 2017/01/07 | | Audio Codec ALC3234 | |
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| | | BAL22 LA-D803P | | A00 | |
| Date: | | Tuesday, June 21, 2016 | | Sheet 18 of 56 | |

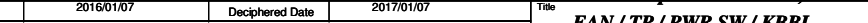
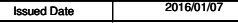
Main Func = WLAN

NGFF WL Con (A Key)



| | | | | | |
|---|------------|------------------------|------------|--------------------------|--|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | |
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| Size | | Document Number | | Rev | |
| | | BAL22 LA-D803P | | A00 | |
| Date: | | Tuesday, June 21, 2016 | | Sheet 20 of 56 | |

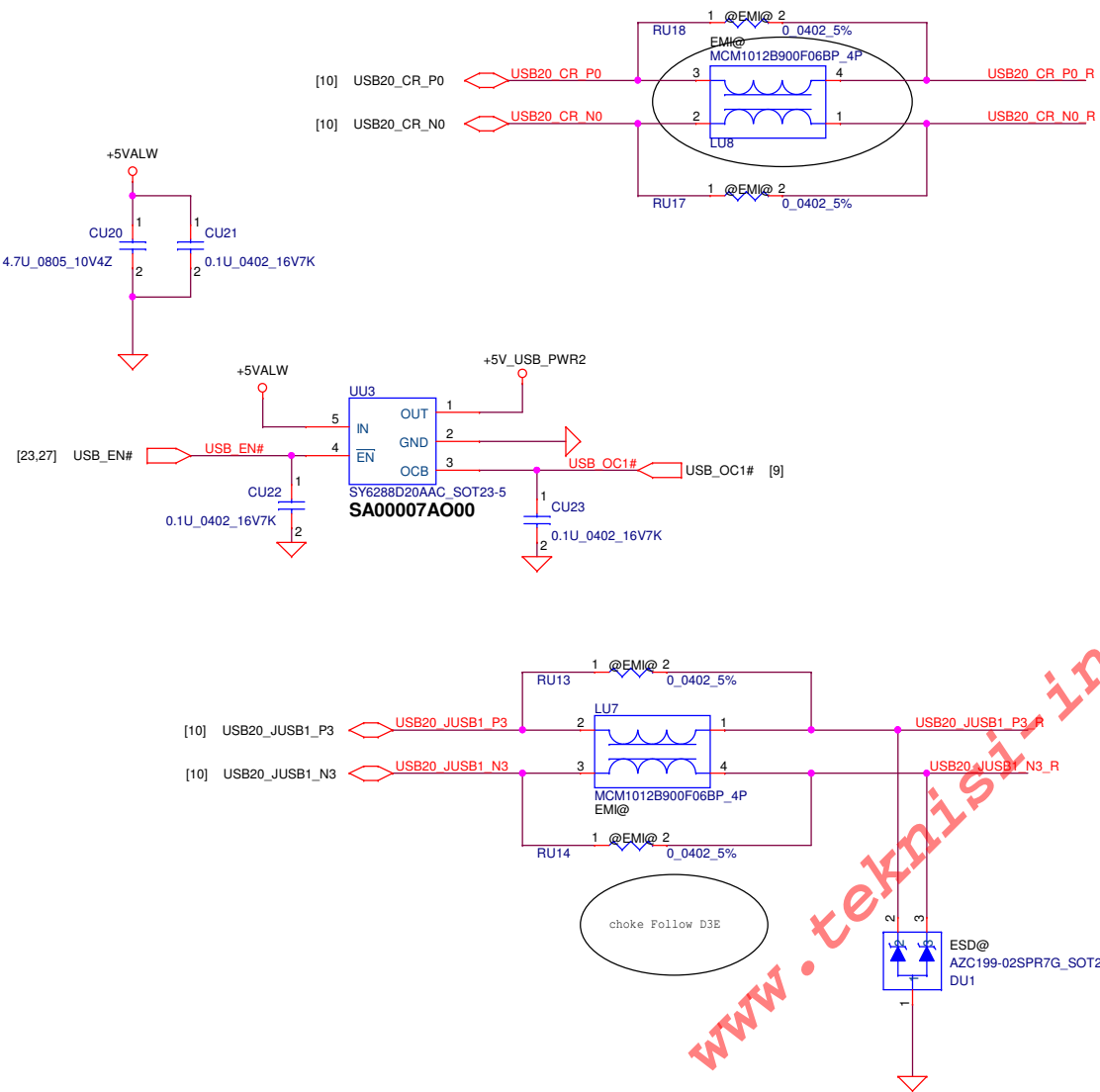
| | | |
|------------|-------|-------------------|
| 2017/01/07 | Title | E4N / TR / BWP SW |
|------------|-------|-------------------|



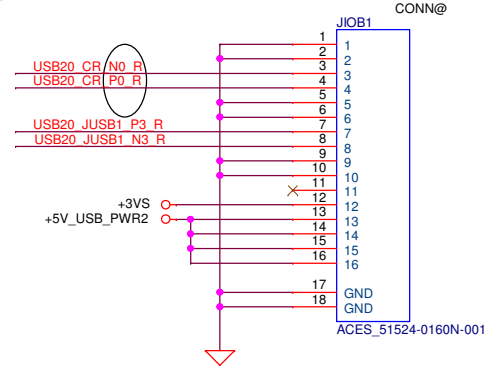
Main Func = IO Connector

IO to MB CONN

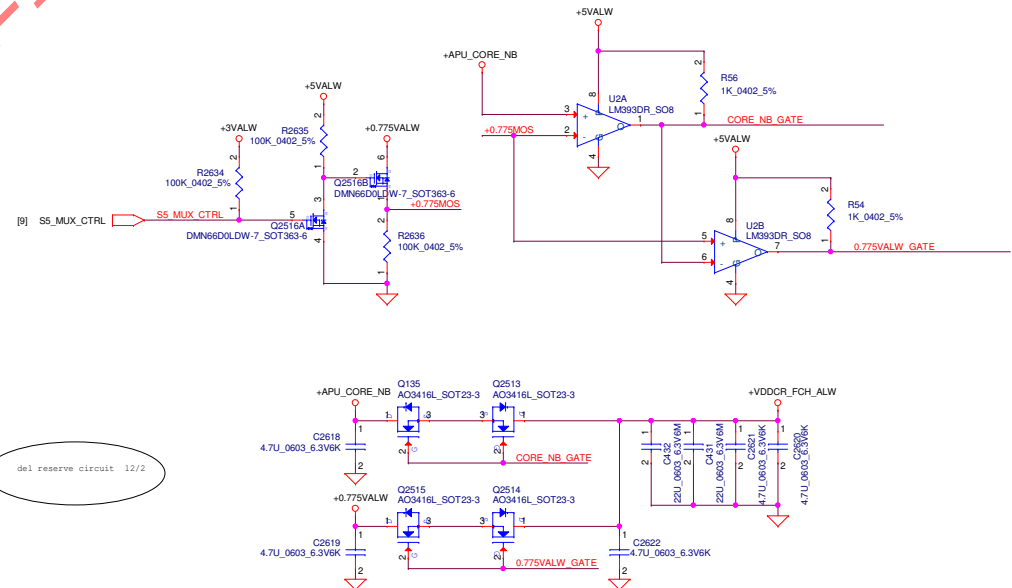
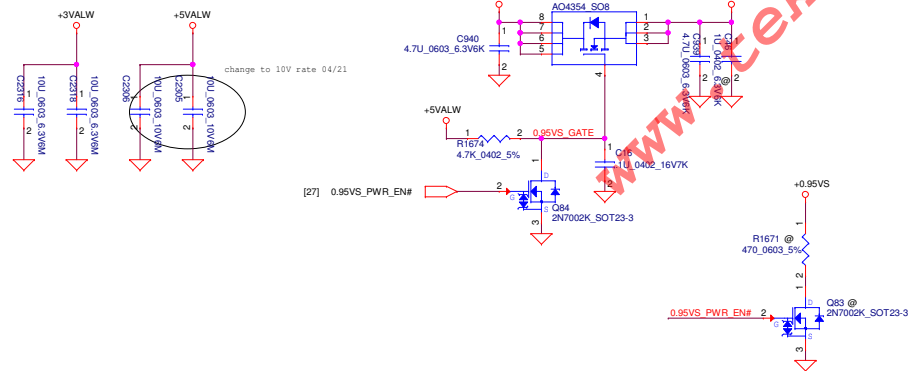
I/O Board Connector



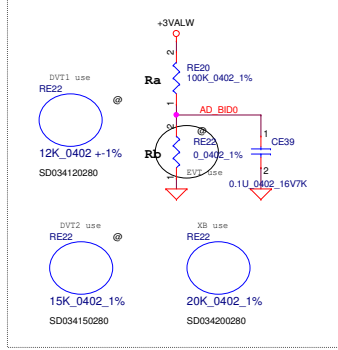
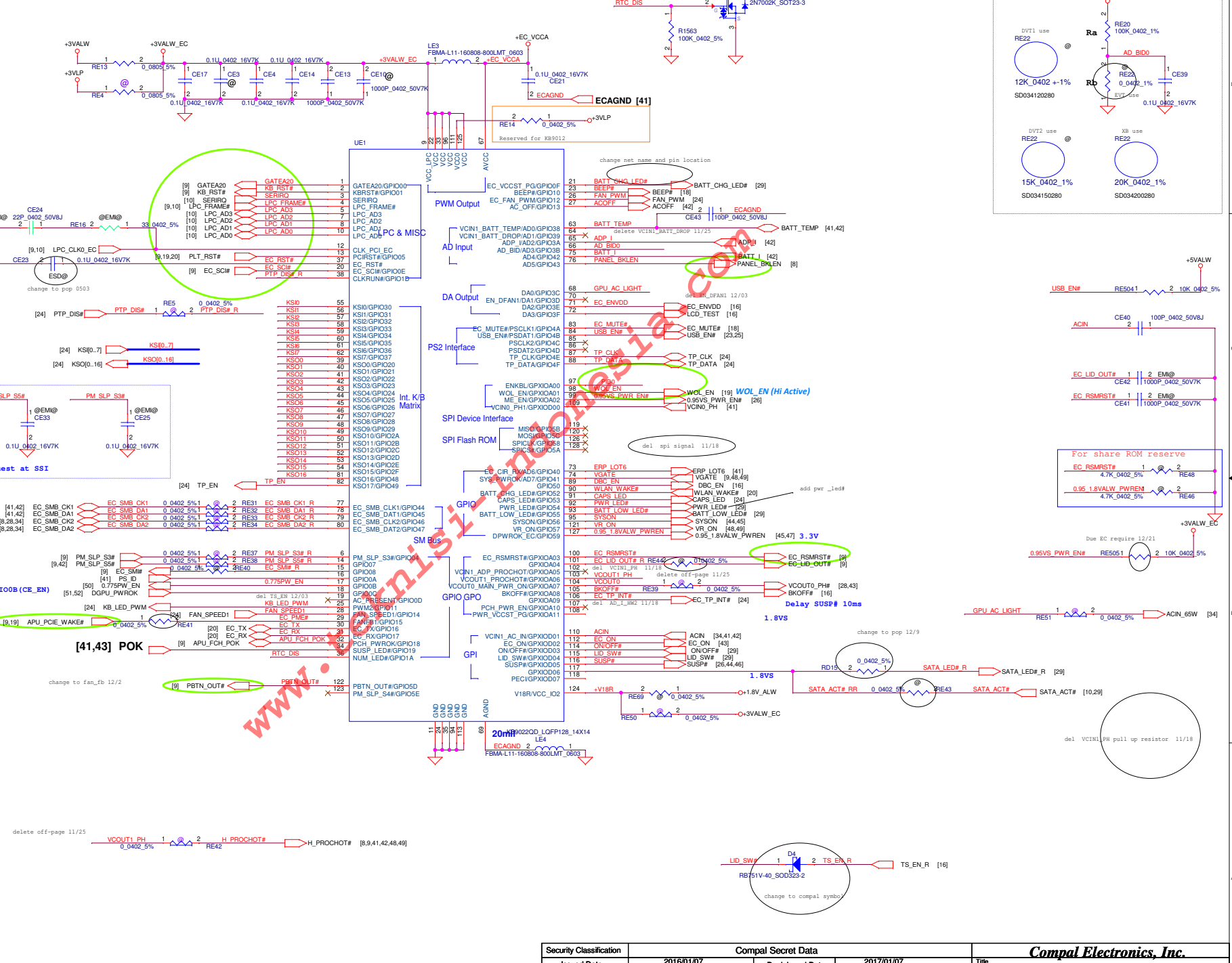
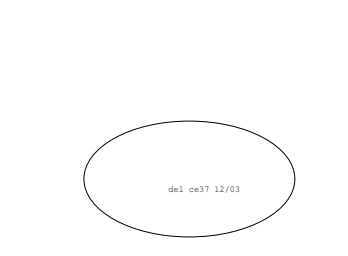
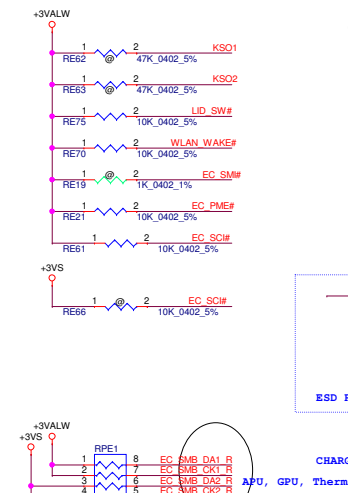
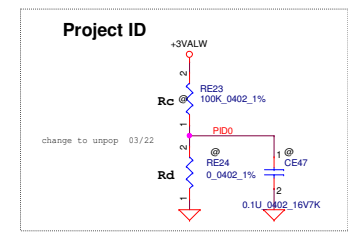
USB2.0
CardReader



| | | | | | |
|---|------------|--------------------|------------|------------------------------|----------------|
| Security Classification | | Compal Secret Data | | Title | |
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | IO-DB | |
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| | | | | BAL22 LA-D803P | A00 |
| | | | | Date: Tuesday, June 21, 2016 | Sheet 25 of 56 |

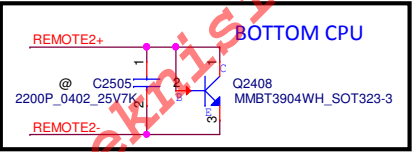
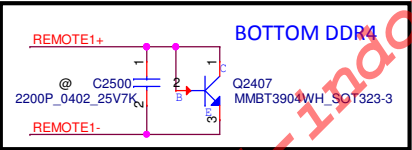
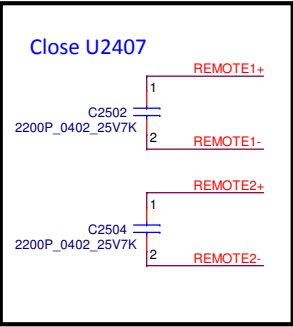
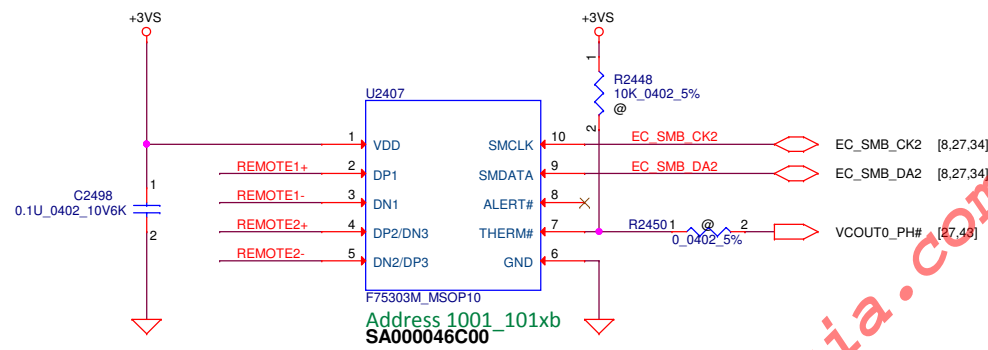


| | | | | | | |
|---|------------|--------------------|------------|--------------------------|-----------------|-------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | | |
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | DC/DC Interface | |
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| | | | | BAL22 LA-D803P | | A00 |
| Date: Tuesday, June 21, 2016 | | | | Sheet | 26 | of 56 |



Main Func = Thermal Sensor

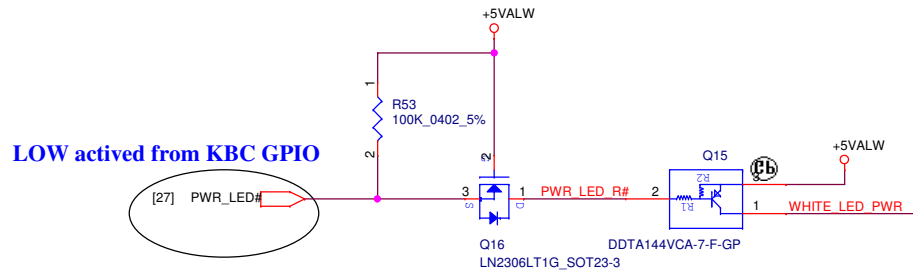
Fintek thermal sensor
placed near by TOP DDR4



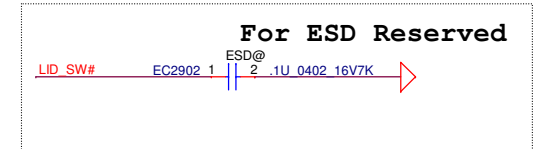
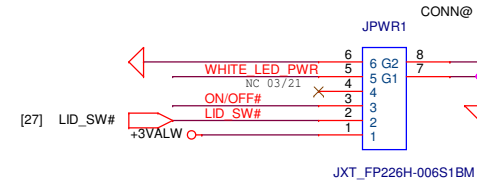
REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

| | | | | | |
|---|------------|--------------------|------------|--------------------------|------------------------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | Thermal Sensor |
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| | | | | Date: | Tuesday, June 21, 2016 |
| | | | | Sheet | 28 of 56 |

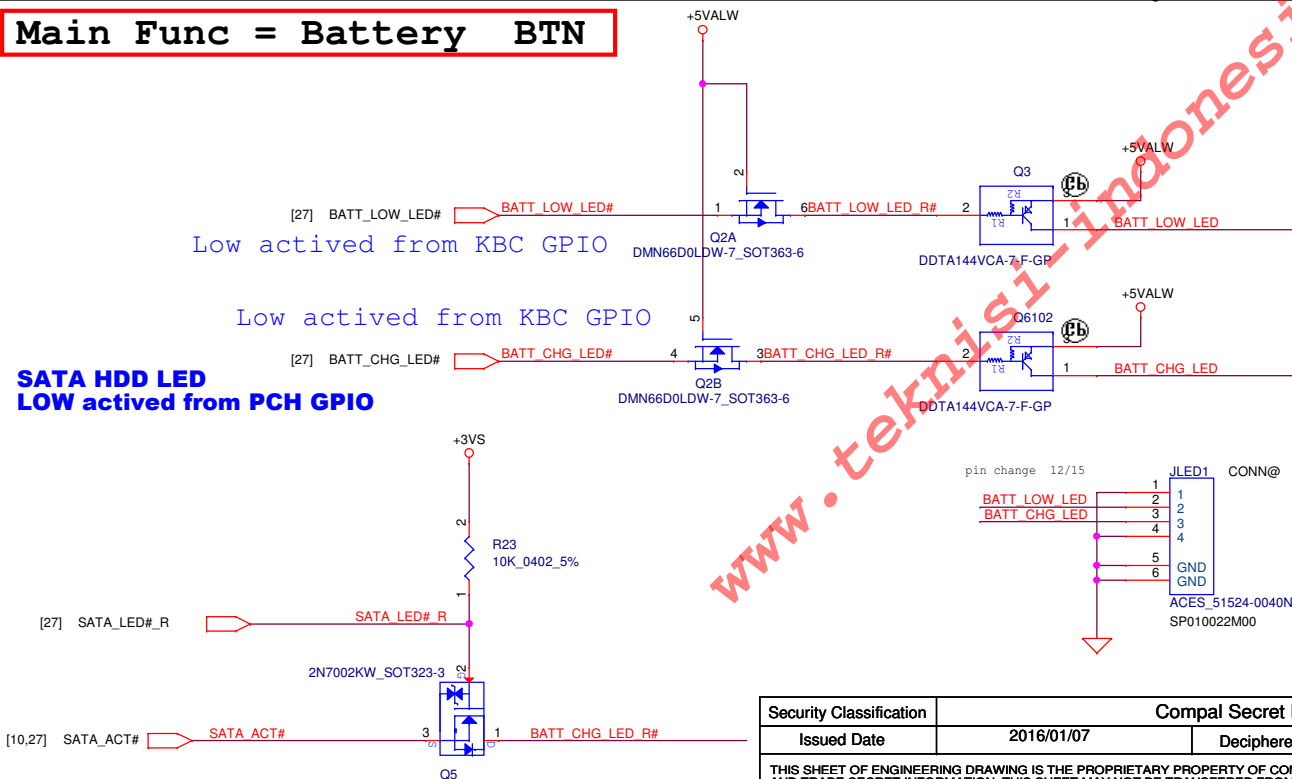
Main Func = POWER BTN



Power button



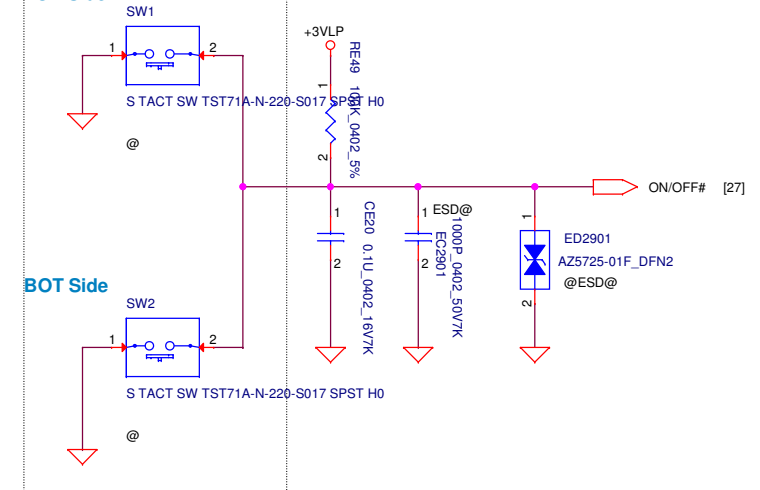
Main Func = Battery BTN



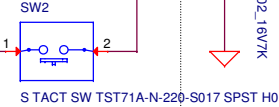
Pop only before MP

ON/OFF switch

TOP Side



BOT Side



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|---|------------|--------------------|------------|--------------------------|------------------------|
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | LED/PWR-DB |
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| | | | | Date | Tuesday, June 21, 2016 |
| | | | | Sheet | 29 of 56 |

Main Func = Screw Hole

ZZZ

| Part Number | Description |
|-------------|---|
| DAZ1PK00100 | PCB BAL22 LA-D803P LS-D802P/D803P/D806P/D807P/D809P |
| PCB_R1@ | |

GCE

ZZZ1

| Part Number | Description |
|-------------|---|
| DAZ1PK00101 | PCB BAL22 LA-D803P LS-D802P-3P/D806P/D807P/D809P GOLD A31 ! |
| PCB_R3G@ | |

ZZZ2

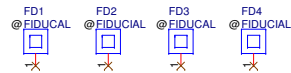
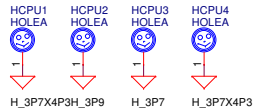
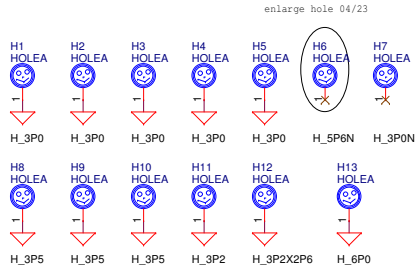
| Part Number | Description |
|-------------|--|
| DAZ1PK00102 | PCB BAL22 LA-D803P LS-D802P-3P/D806P-7P/D809P TRiPOD A31 ! |
| PCB_R3T@ | |

TRiPOD

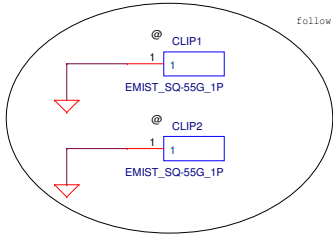
ZZZ3

| Part Number | Description |
|-------------|---|
| DAZ1PK00103 | PCB BAL22 LA-D803P LS-D802P-3P/D806P-7P/9P HANNSTAR A31 ! |
| PCB_R3H@ | |

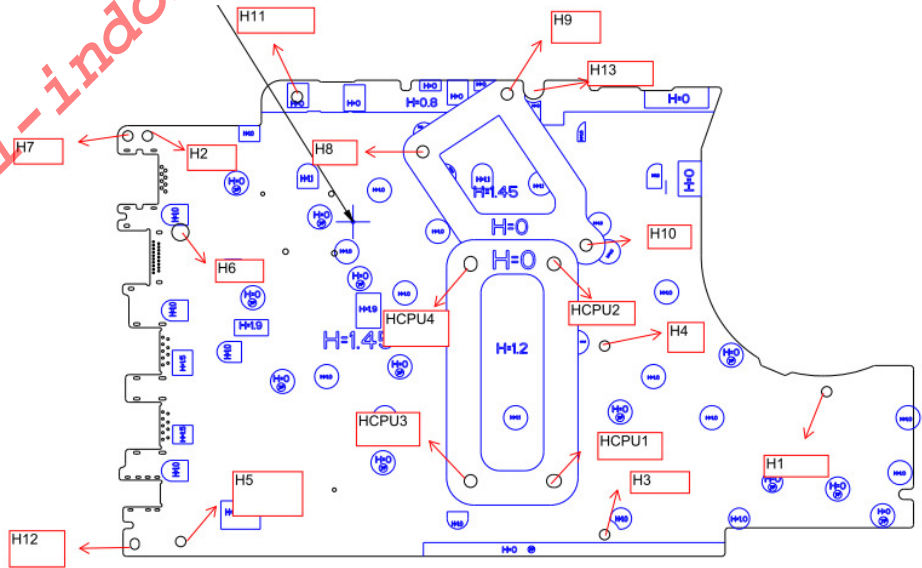
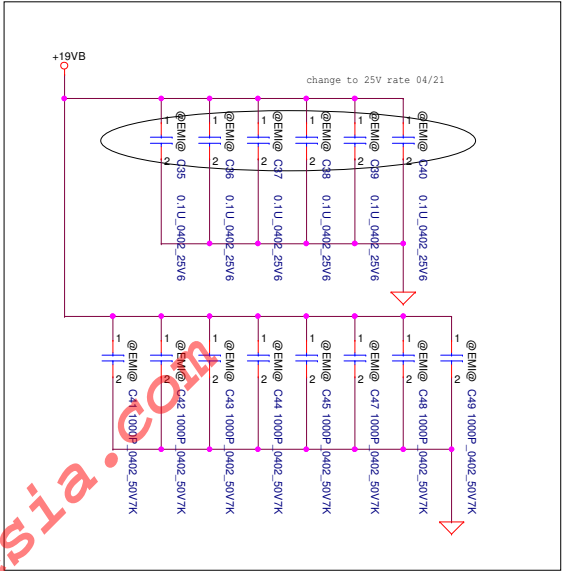
HANNSTAR



del FD5 FD6 12/1



follow EMI require 12/15



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| | | | | Rev |
| | | | | A00 |
| | | | | Date: Tuesday, June 21, 2016 |
| | | | | Sheet 30 of 56 |

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2016/02/24

EC Pin 110 Input

EC Pin 112 Output

EC Pin 34 Input

EC Pin 127 Output

EC Pin 114 Input

EC Pin 100 Output

EC Pin 122 Output

EC Pin 14 Input

EC Pin 6 Input

EC Pin 95 Output

EC Pin 116 Output

EC Pin 99 Output

EC Pin 121 Output

EC Pin 74 Input

(APU Input) EC Pin 32 Output

(APU Output) EC Pin 108 Input

(APU Output) EC Pin 13 Input

(APU Output) APU_PCIE_RST#

(APU Output) EC Pin 118 Input

(APU Output)

(APU Output)

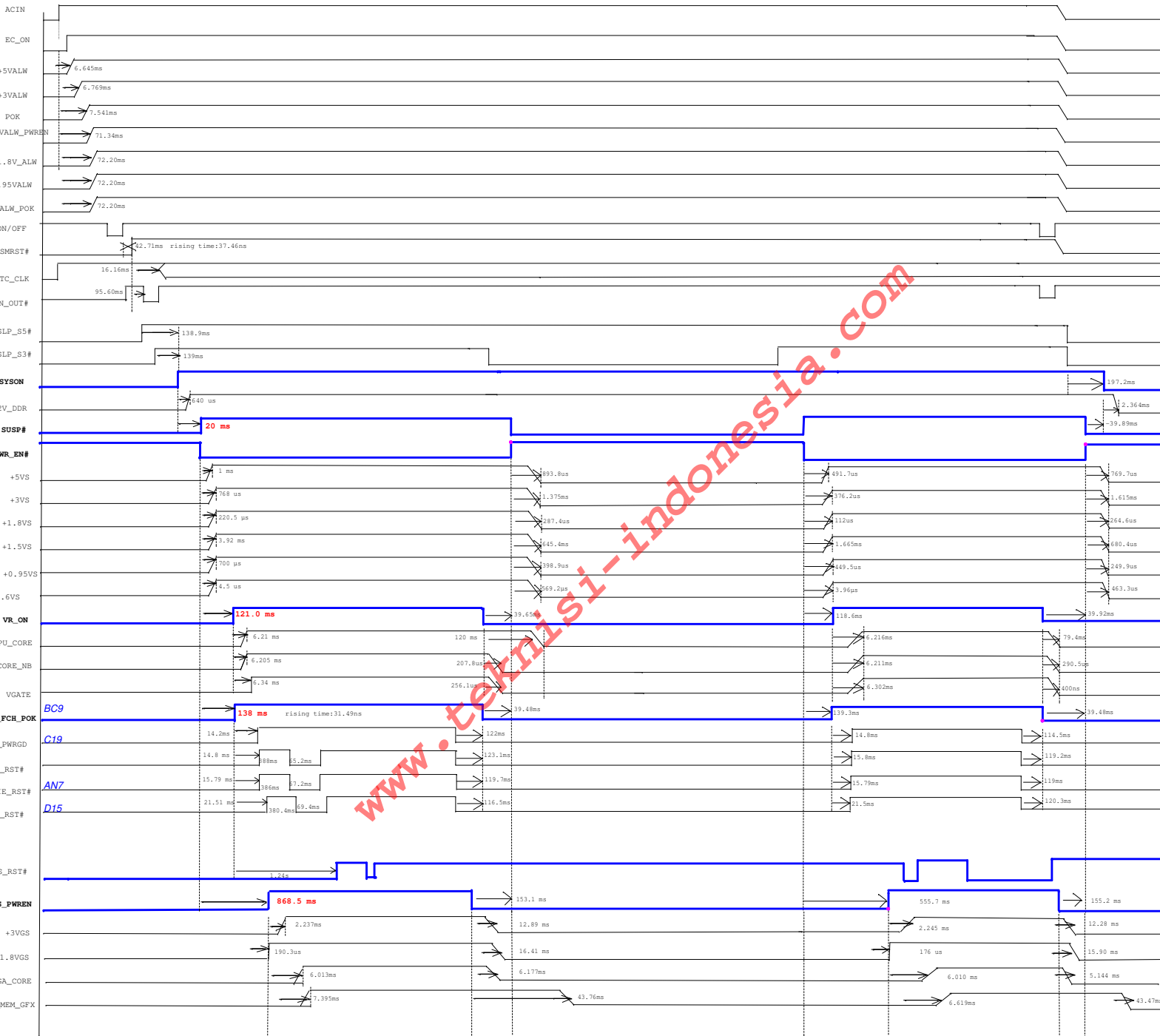
<20ms

Boot

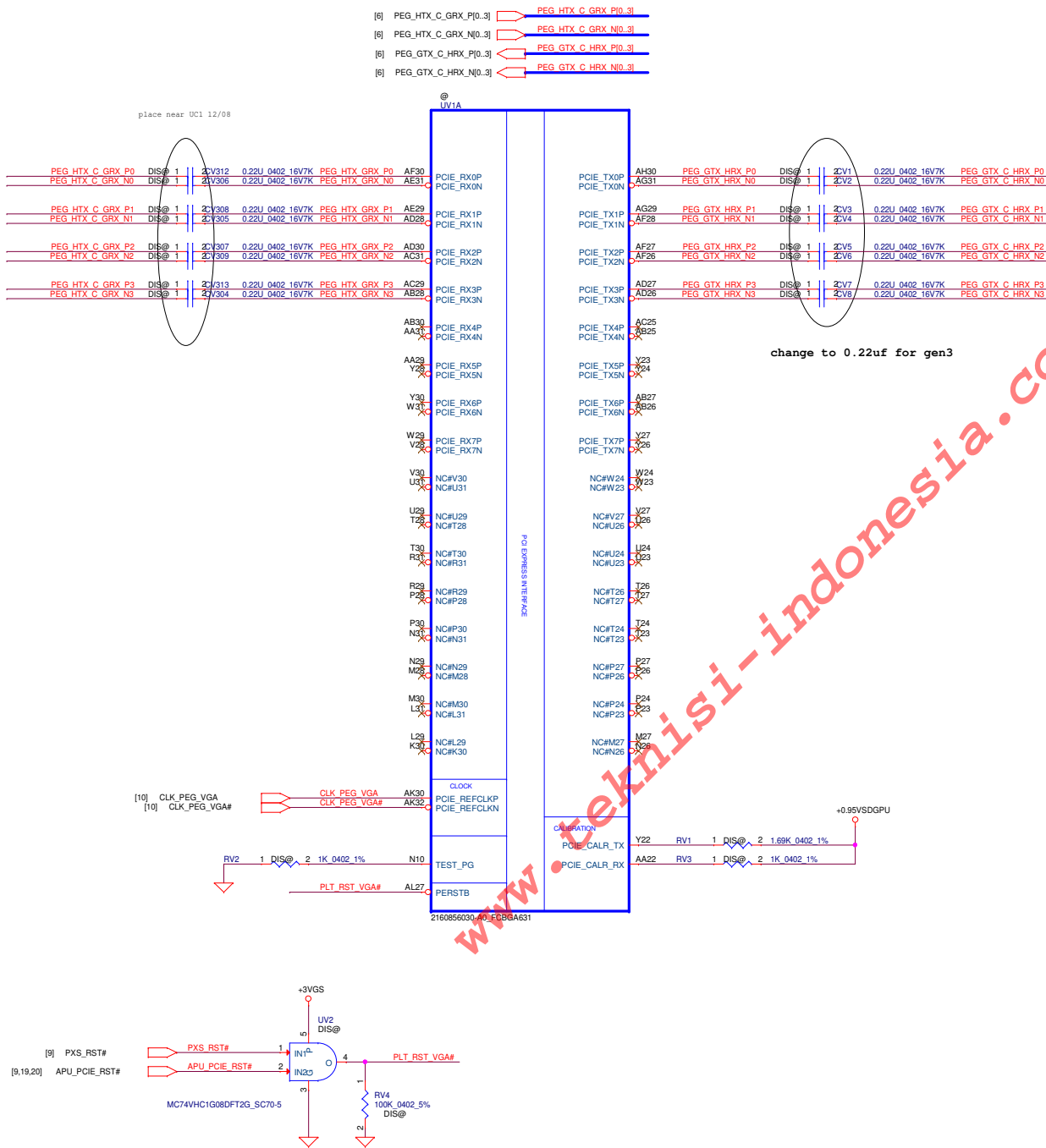
Enter S3

S3 Resume

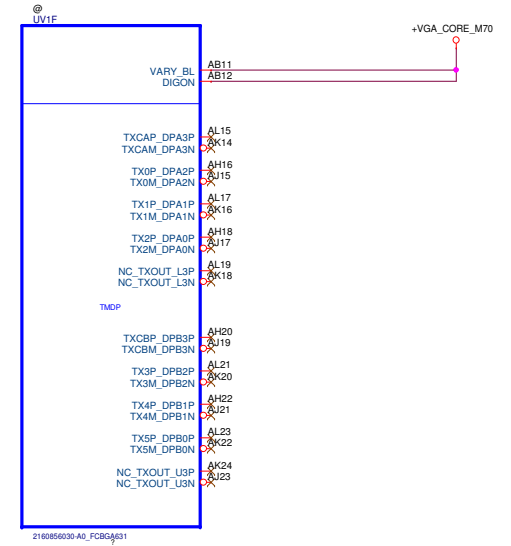
Shut Down



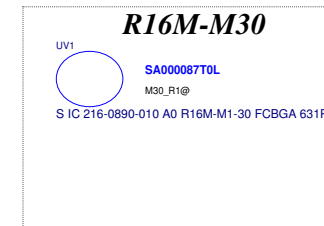
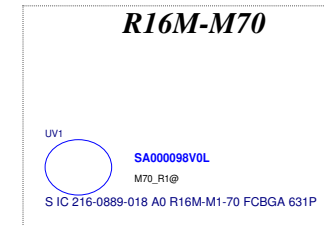
| | | | | | |
|---|--------------------|-----------------|------------|--------------------------|------------------------|
| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | |
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | S5 MUX CTRL |
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| | | | | Rev | A00 |
| | | | | Date | Tuesday, June 21, 2016 |
| | | | | Sheet | 32 of 56 |



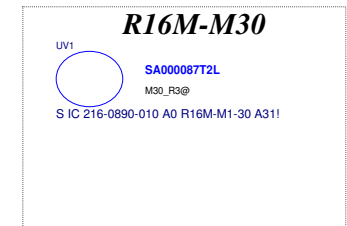
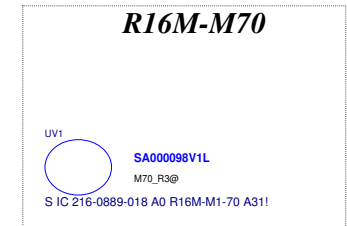
No Use GPU Display Port output



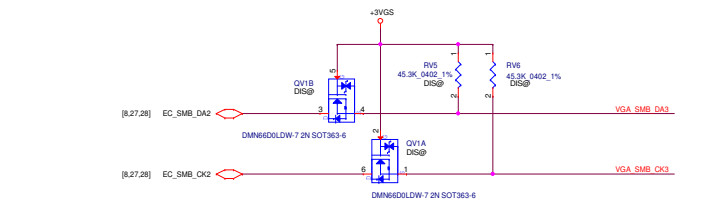
GPU R1



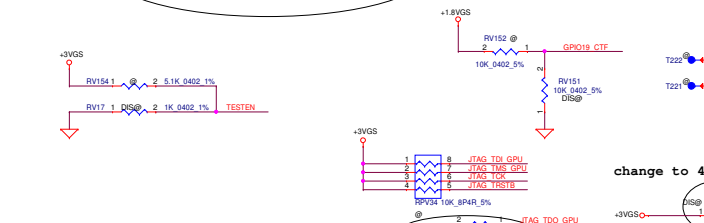
GPU R3



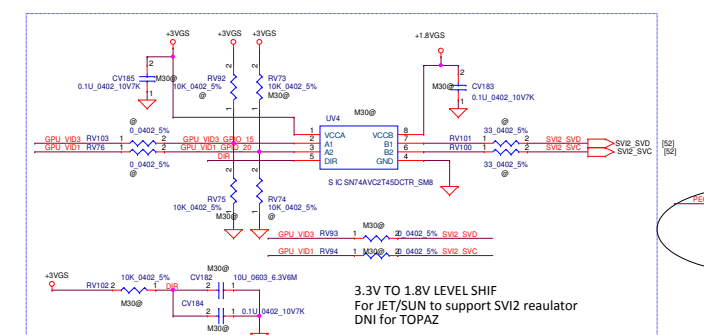
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
|---|------------|--------------------|------------|--------------------------|------------------------|
| Issued Date | 2016/01/07 | Deciphered Date | 2017/01/07 | Title | M30/M70_PCIE/DP |
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| | | | | Sheet | 33 of 56 |
| | | | | Date | Tuesday, June 21, 2016 |
| | | | | Rev | A00 |



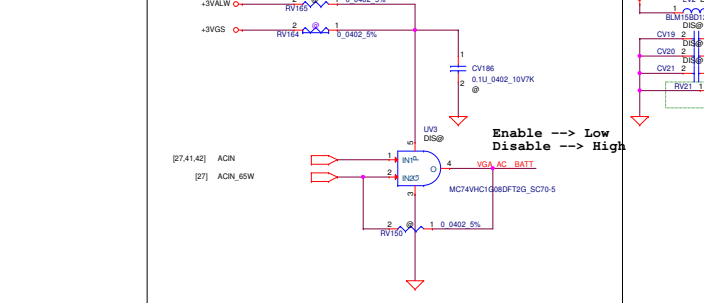
del thermal sensor 11/19



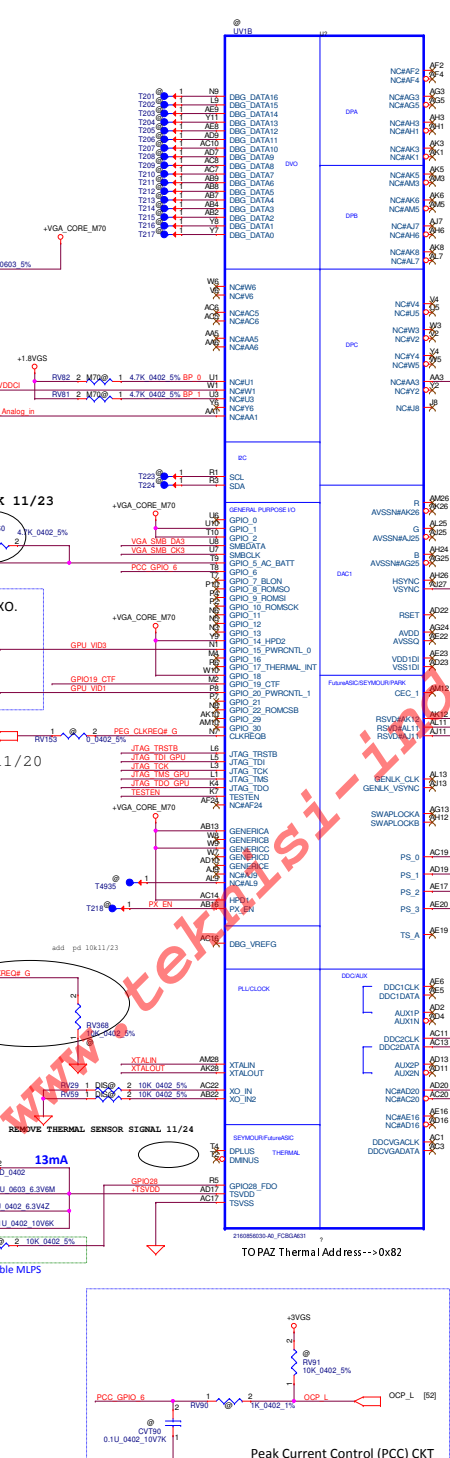
reserve level shift colay resistor 11/20



ADD GPU POWER SAVING MODE 11/26



Enable --- Low
Disable --- High



Resistor Divider Lookup Table
0402 1% resistors are equired

| R_pu (ohm) | R_pd (ohm) | Bitd [3:1] |
|------------|------------|------------|
| NC | 4.75k | 000 |
| 8.45k | 2k | 001 |
| 4.53k | 2k | 010 |
| 6.98k | 4.99k | 011 |
| 4.53k | 4.99k | 100 |
| 3.24k | 5.62k | 101 |
| 3.4k | 10k | 110 |
| 4.75k | NC | 111 |

Capacitor Divider Lookup Table

| Cap (nF) | Bitd [5:4] |
|----------|------------|
| 680nF | 00 |
| 82nF | 01 |
| 10nF | 10 |
| NC | 11 |

change bom structure to disc 11/24

change bom structure to disc 11/24

change bom structure to disc 11/24

change bom structure to disc 11/24

change bom structure to disc 11/24

change bom structure to disc 11/24

change bom structure to disc 11/24

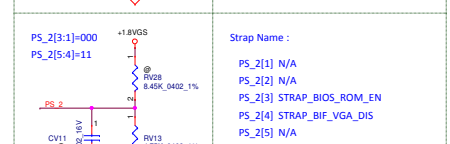
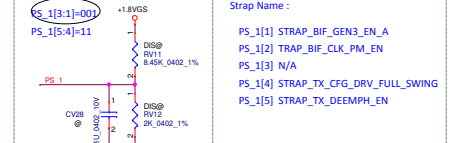
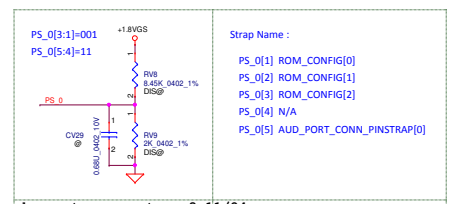
change bom structure to disc 11/24

change bom structure to disc 11/24

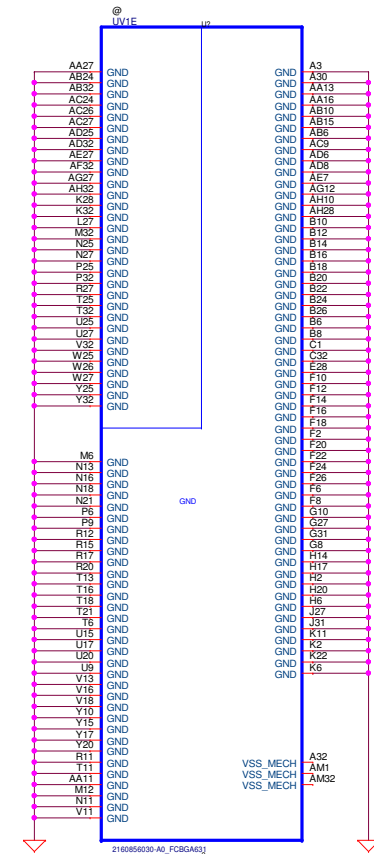
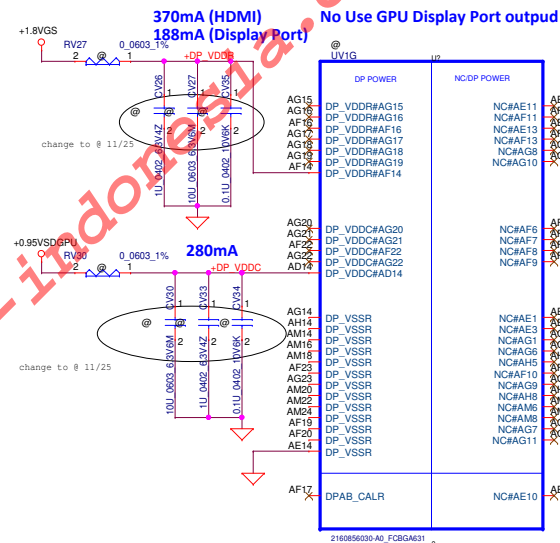
change bom structure to disc 11/24

change bom structure to disc 11/24

change bom structure to disc 11/24



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| Date | | Tuesday, June 21, 2016 | | Sheet | | 35 of 56 | | | | | |

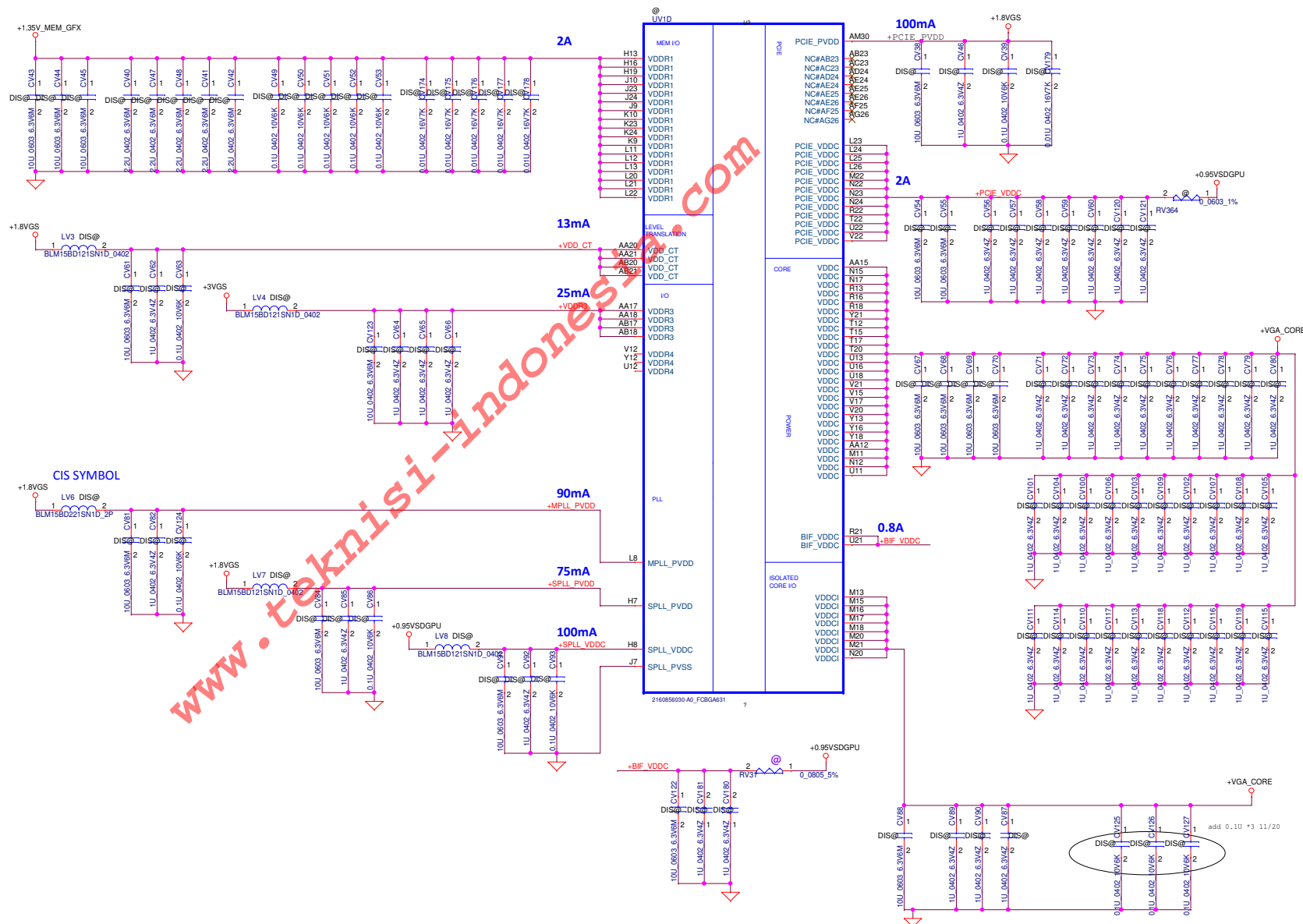
| | | | |
|---------------------------------------|-------------|------------|--------------|
| +VGA_CORE | 10uF | 1uF | 0.1uF |
| VDDC VDDC and VDDCI TDC 28A | 4 | 30 | 0 |
| VDDCI | 1 | 3 | 3 |

| | | | |
|-----------------|------|-----|-------|
| +0.95VSDGPU | 10uF | 1uF | 0.1uF |
| PCIE_VDDC 2A | 2 | 7 | 0 |
| BIF_VDDC 0.8A | 1 | 2 | 0 |
| SPLL_VDDC 100mA | 1 | 1 | 1 |

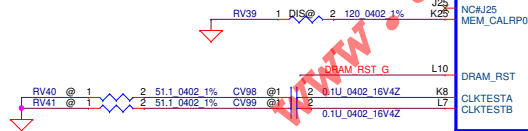
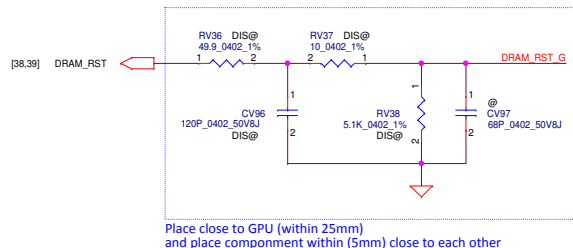
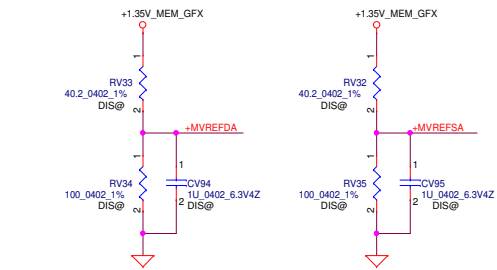
| | | | | |
|----------------|------|-------|-------|--------|
| +1.35V_MEM_GFX | 10uF | 2.2uF | 0.1uF | 0.01uF |
| VDDR1_2A | 3 | 5 | 5 | 5 |

| +1.8VGS | | 10uF | 1uF | 0.1uF | 0.01uF |
|-----------|-------|------|------|-------|--------|
| PCIE_PVDD | 100mA | 1 | 1 | 1 | 1 |
| MPLL_PVDD | 90mA | 1 | 1 | 1 | 0 |
| SPLL_PVDD | 75mA | 1 | 1 | 1 | 0 |
| VDD_CT | 13mA | 1 | 1 | 1 | 0 |
| +DP_VDDR | 40mA | 1(@) | 1(@) | 1(@) | 0 |
| +DP_VDDC | | 1(@) | 1(@) | 1(@) | 0 |

| | | | |
|------------|------|-----|-------|
| +3VGS | 10uF | 1uF | 0.1uF |
| VDDR3 25mA | 1 | 3 | 0 |

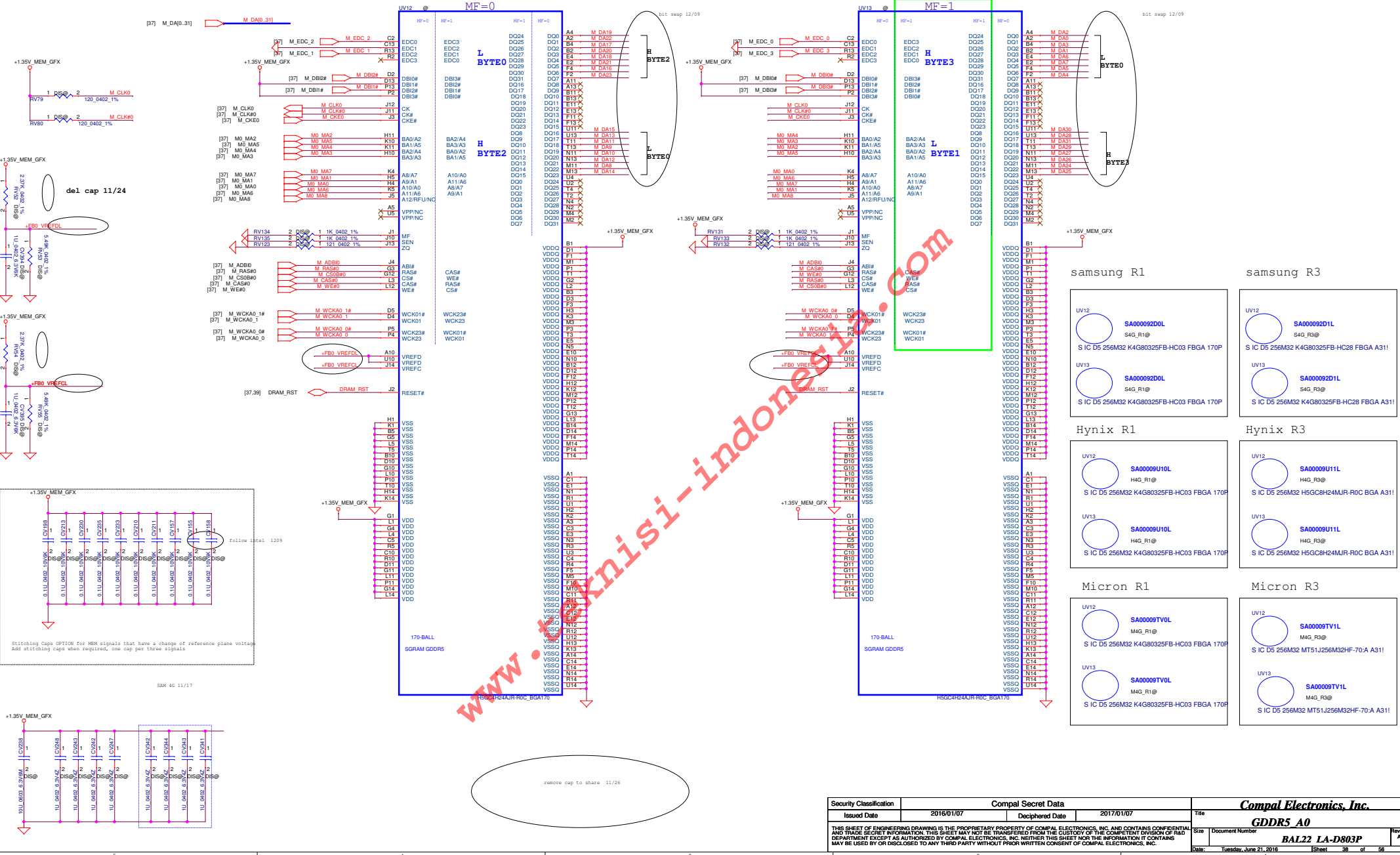


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| | | | | | Custom | BAL22_1A-D803P | AC |
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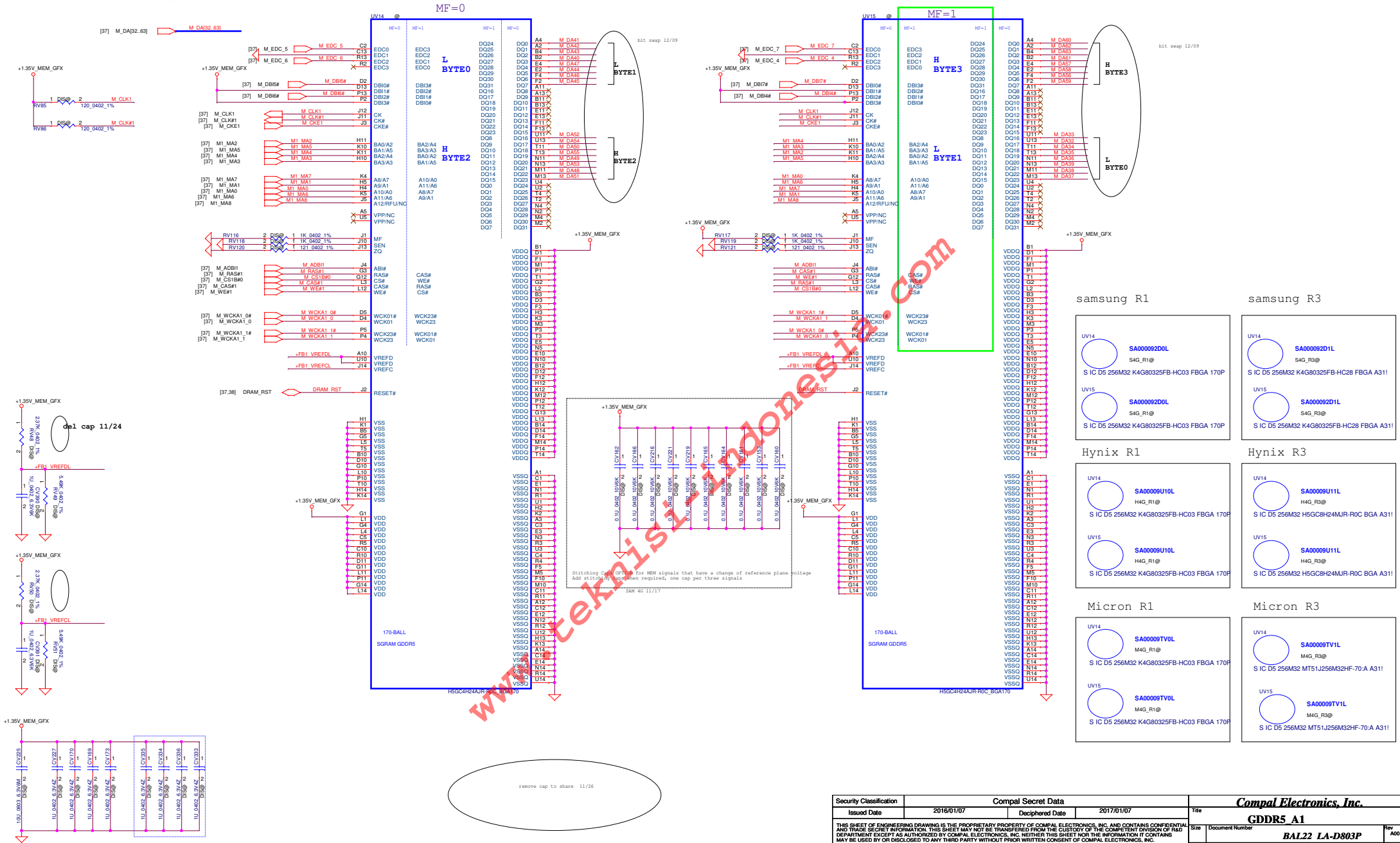
| GPIOs/IOs | | GPIOs/IOs | |
|-----------|-----|------------------|-----|
| M_DA0 | K27 | MAA0_0/MAA_0 | K17 |
| M_DA1 | J29 | MAA0_1/MAA_1 | J20 |
| M_DA2 | H30 | MAA0_2/MAA_2 | H23 |
| M_DA3 | H32 | MAA0_3/MAA_3 | G23 |
| M_DA4 | G29 | MAA0_4/MAA_4 | G24 |
| M_DA5 | F28 | MAA0_5/MAA_5 | H24 |
| M_DA6 | F32 | MAA0_6/MAA_6 | J18 |
| M_DA7 | F30 | MAA0_7/MAA_7 | K19 |
| M_DA8 | C30 | MAA0_8/MAA_8 | G20 |
| M_DA9 | F27 | MAA0_9/MAA_9 | L17 |
| M_DA10 | A28 | MAA1_0/MAA_0 | J14 |
| M_DA11 | C28 | MAA1_1/MAA_1 | J11 |
| M_DA12 | E27 | MAA1_2/MAA_2 | J13 |
| M_DA13 | G26 | MAA1_3/MAA_3 | H11 |
| M_DA14 | D26 | MAA1_4/MAA_4 | G11 |
| M_DA15 | F25 | MAA1_5/MAA_5 | J18 |
| M_DA16 | A25 | MAA1_6/MAA_6 | L15 |
| M_DA17 | C25 | MAA1_7/MAA_7 | G14 |
| M_DA18 | E25 | MAA1_8/MAA_8 | L16 |
| M_DA19 | D24 | MAA1_9/RSVD | K |
| M_DA20 | E23 | WCKA0_0/DQMA0_0 | E32 |
| M_DA21 | F23 | WCKA0_0/DQMA0_1 | E30 |
| M_DA22 | D22 | WCKA0_1/DQMA0_2 | A21 |
| M_DA23 | F21 | WCKA0B_1/DQMA0_3 | E13 |
| M_DA24 | E21 | WCKA1_0/DQMA1_0 | D12 |
| M_DA25 | D20 | WCKA1B_0/DQMA1_1 | E3 |
| M_DA26 | F19 | WCKA1_1/DQMA1_2 | F4 |
| M_DA27 | A19 | WCKA1B_1/DQMA1_3 | H28 |
| M_DA28 | D18 | EDCA0_0/QSA0_0 | C27 |
| M_DA29 | F17 | EDCA0_1/QSA0_1 | A23 |
| M_DA30 | A17 | EDCA0_2/QSA0_2 | E19 |
| M_DA31 | C17 | EDCA0_3/QSA0_3 | D10 |
| M_DA32 | E17 | EDCA1_0/QSA1_0 | D6 |
| M_DA33 | D16 | EDCA1_2/QSA1_2 | G5 |
| M_DA34 | F15 | EDCA1_3/QSA1_3 | H27 |
| M_DA35 | A15 | DBBIA0_0/QSA0_0B | A27 |
| M_DA36 | D14 | DBBIA0_1/QSA0_1B | C23 |
| M_DA37 | F13 | DBBIA0_2/QSA0_2B | G19 |
| M_DA38 | A13 | DBBIA0_3/QSA0_3B | E15 |
| M_DA39 | C13 | DBBIA1_0/QSA1_0B | E9 |
| M_DA40 | E11 | DBBIA1_1/QSA1_1B | C5 |
| M_DA41 | A11 | DBBIA1_2/QSA1_2B | H4 |
| M_DA42 | C11 | DBBIA1_3/QSA1_3B | L18 |
| M_DA43 | F11 | ADBIA0/ODTA0 | K16 |
| M_DA44 | A9 | ADBIA1/ODTA1 | H26 |
| M_DA45 | C9 | CLKA0 | H25 |
| M_DA46 | F9 | CLKA0B | G9 |
| M_DA47 | D8 | CLKA1 | G8 |
| M_DA48 | E7 | CLKA1B | G22 |
| M_DA49 | A7 | RASA0B | G17 |
| M_DA50 | C7 | RASA1B | G19 |
| M_DA51 | F7 | CASA0B | G16 |
| M_DA52 | A5 | CASA1B | H22 |
| M_DA53 | E5 | CSA0B_0 | J22 |
| M_DA54 | C3 | CSA0B_1 | K13 |
| M_DA55 | E1 | CSA1B_0 | K20 |
| M_DA56 | G7 | CSA1B_1 | J17 |
| M_DA57 | G6 | CKEA0 | G25 |
| M_DA58 | G1 | CKEA1 | H10 |
| M_DA59 | G3 | WEA0B | |
| M_DA60 | J6 | WEA1B | |
| M_DA61 | J1 | | |
| M_DA62 | J3 | | |
| M_DA63 | J5 | | |
| +MVREFDA | K26 | | |
| +MVREFSA | L26 | | |

clamshell configuration 11/26



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clamshell configuration 11/26



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| GDDR5 A1 | | Rev A00 | |
| Size | Document Number | BAL22 LA-D803P | |
| Date | Tuesday, June 21, 2016 | Sheet | 39 of 56 |

Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.
2. It is recommended that the 3.3-V rail ramp up first.
3. It is recommended that the 0.95-V rail reach at least 90% of its nominal value no later than 2 ms from the start of VDDC ramping up.
4. The power rails that are shared with other components on the system should be gated for dGPU use only when the dGPU is powered down (for example AMD PowerXpress® idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ? 50 mV/μs).
5. VDDOC and VDDT_C should not ramp up simultaneously. For example, VDDC should reach 90% before VDDT_C starts to ramp up (or vice versa).
6. For power down, reversing the ramp-up sequence is recommended.

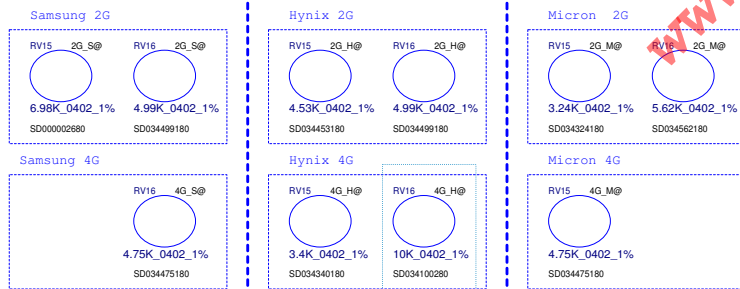
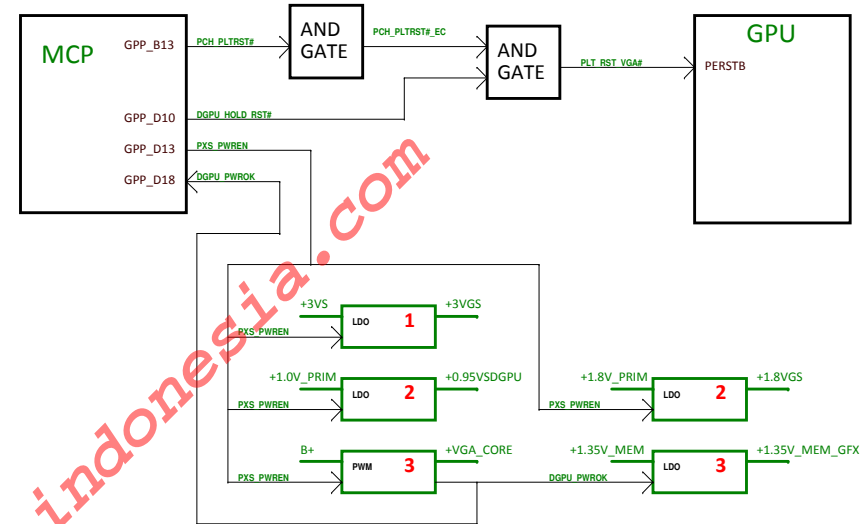
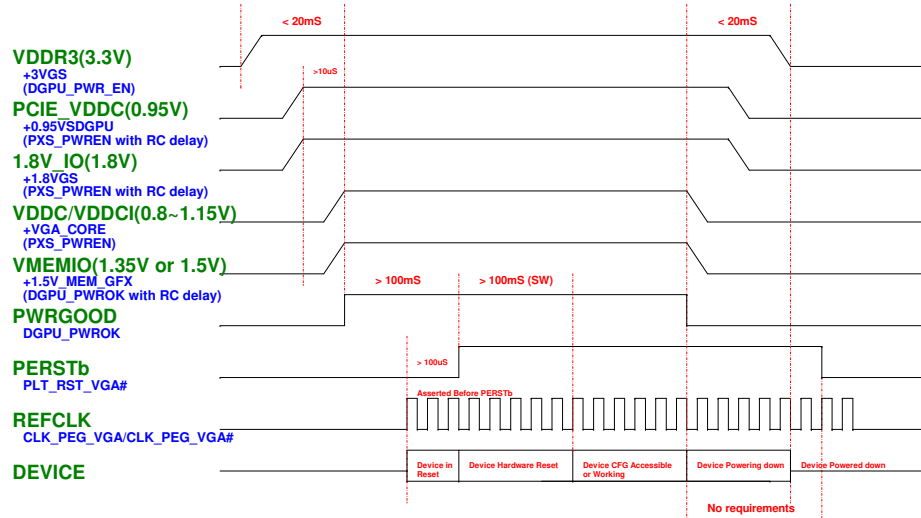


Table 3-21 Resistor Divider Lookup Table

| R _{pu} (Ω) | R _{pd} (Ω) | Bits [3:1] |
|---------------------|---------------------|------------|
| NC | 4750 | 000 |
| 8450 | 2000 | 001 |
| 4530 | 2000 | 010 |
| 6980 | 4990 | 011 |
| 4530 | 4990 | 100 |
| 3240 | 5620 | 101 |
| 3400 | 10000 | 110 |
| 4750 | NC | 111 |

Note: 0402 1% resistors are required.

For AMD R16M-M30/M70 VRAM Only

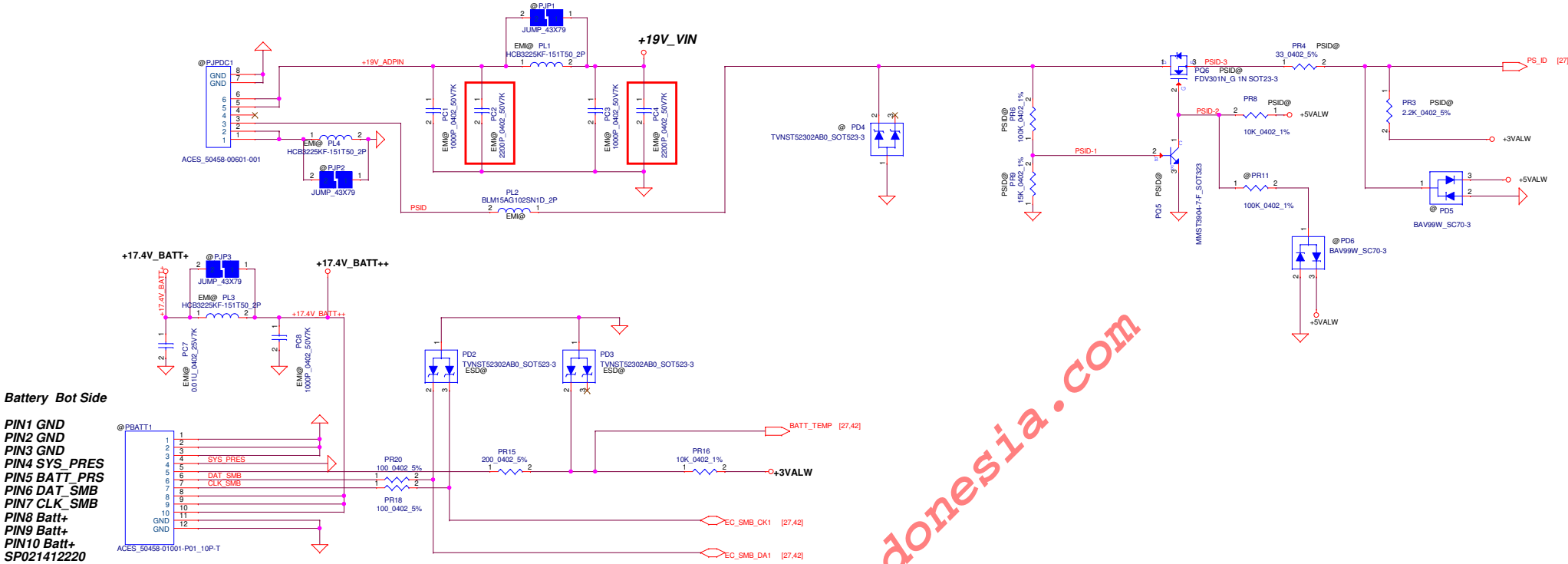
| Memory ID | R3 P/N | Vendor | Configuration | Size |
|-----------|-------------|---------|--------------------|------|
| 100 | SA00009U10L | Hynix | H5GC8H24MJR-R0C | 2GB |
| 011 | SA000092D0L | SAMSUNG | K4G80325FB-HC28 | 2GB |
| 101 | SA00009TV0L | Micron | MT51J256M32HF-70:A | 2GB |

| Memory ID | R3 P/N | Vendor | Configuration | Size |
|-----------|-------------|---------|--------------------|------|
| 110 | SA00009U10L | Hynix | H5GC8H24MJR-R0C | 4GB |
| 000 | SA000092D0L | SAMSUNG | K4G80325FB-HC28 | 4GB |
| 111 | SA00009TV0L | Micron | MT51J256M32HF-70-A | 4GB |

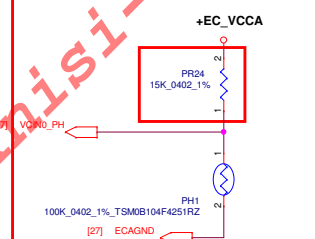
Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 GND
PIN4 SYS_PRES
PIN5 BATT_PRS
PIN6 DAT_SMB
PIN7 CLK_SMB
PIN8 Batt+
PIN9 Batt+
PIN10 Batt+
SP021412220

Other component (37.1)
ACES_50458-01001-P01_10P-T

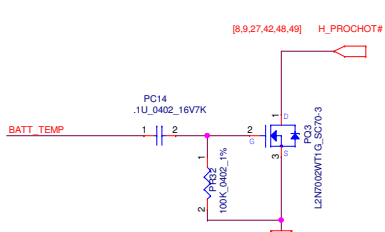


PH1 under CPU bottom side :
CPU thermal protection at 92 +/- 3 degree C



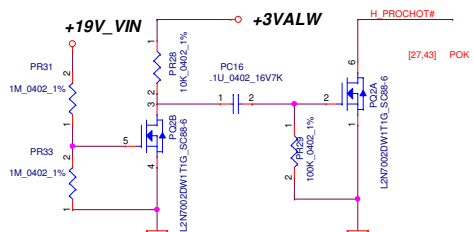
Adapter protection:

if battery removed, adaptor only,
then trigger the H_PROCHOT#,
keep @ in BOM since battery can not
be removed by end user

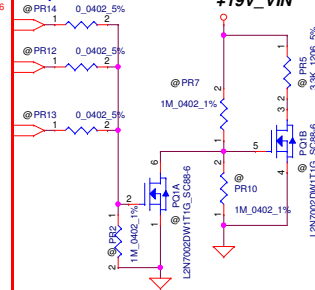


Battery protection:

asserts H_PROCHOT# when adaptor is
unplugged, keep low for 10ms
till SW PROCHOT# is issued by EC



Erp lot6 Circuit

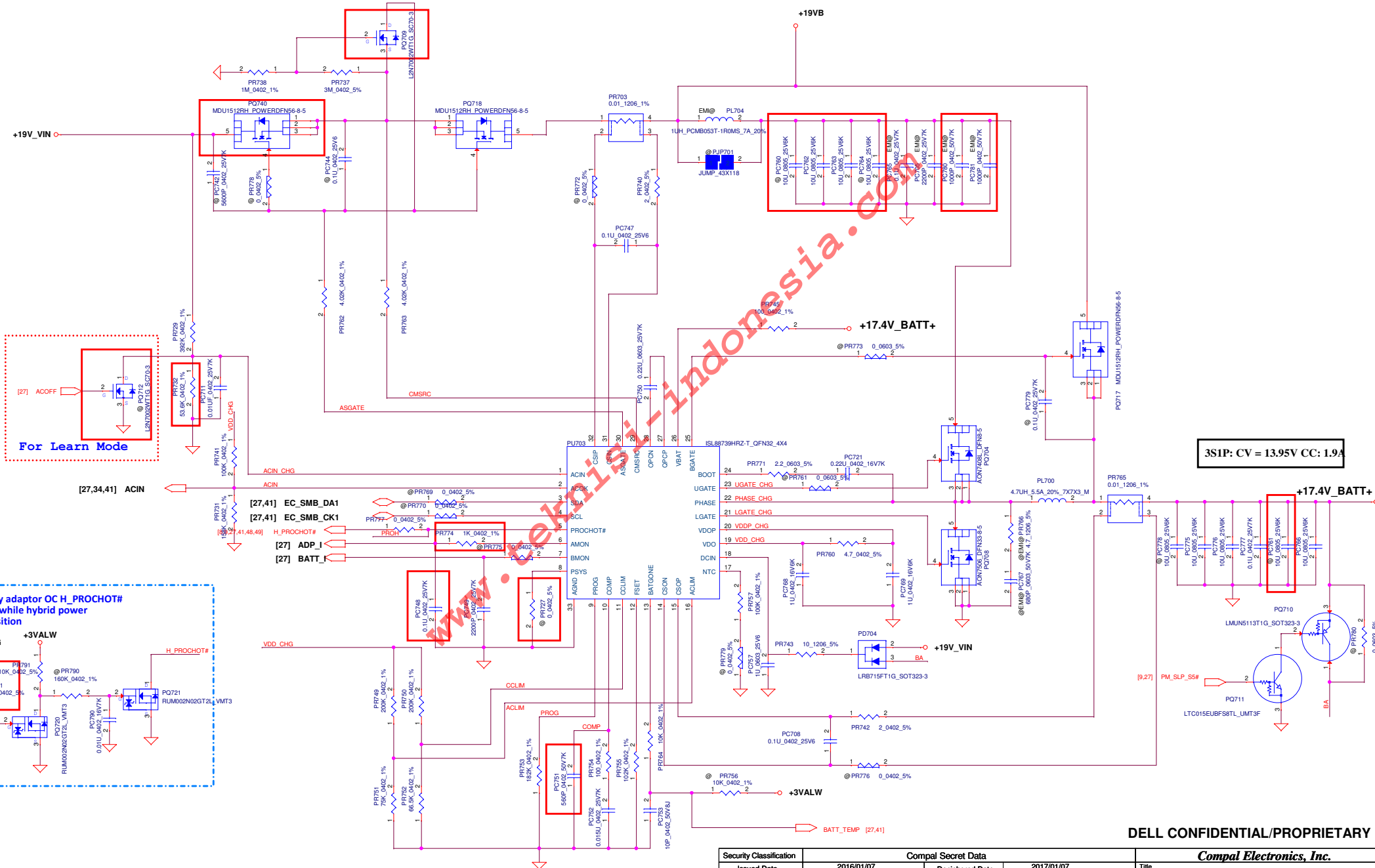


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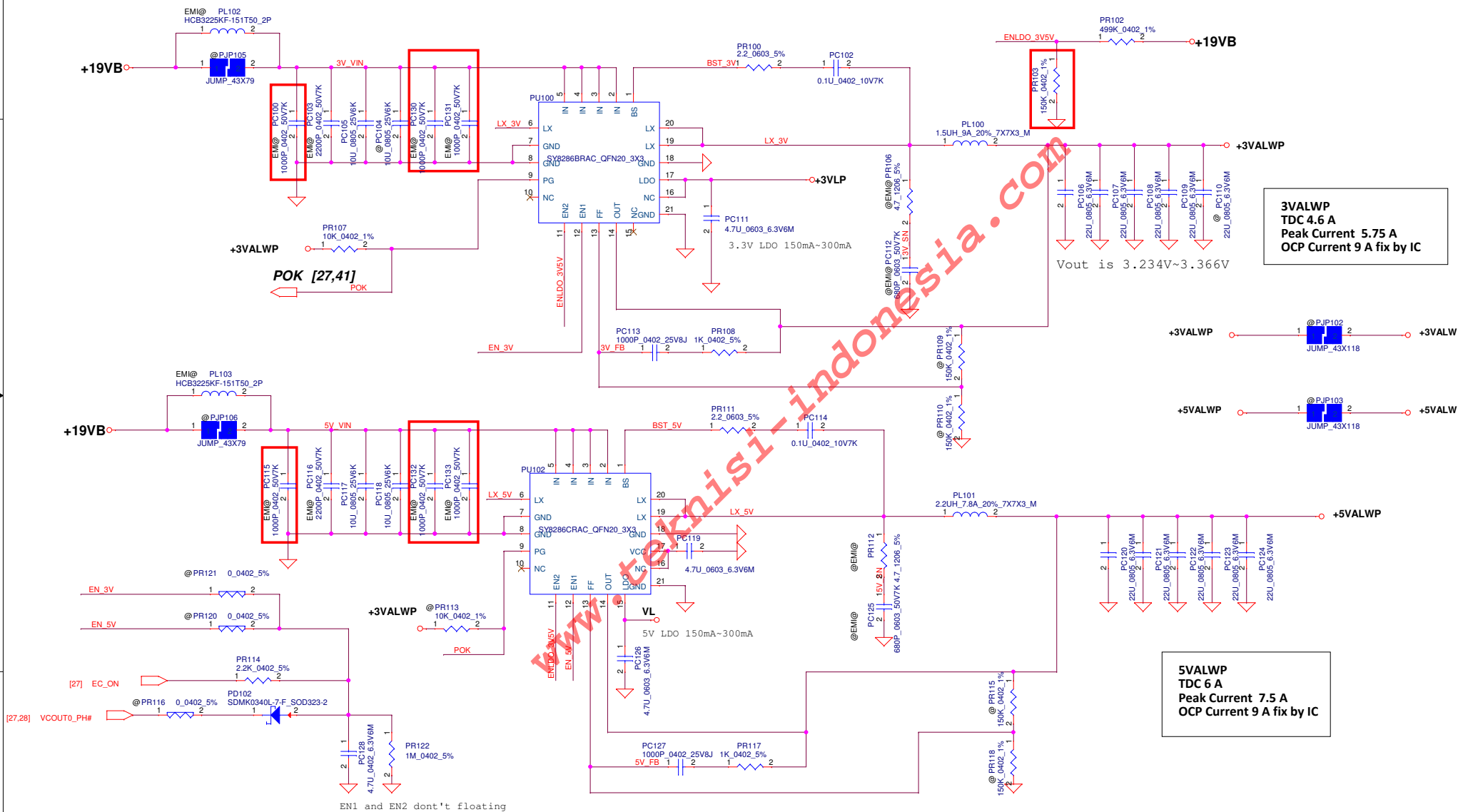
$I_{ada}=0\sim2.30A(45W)$

$$ADP_I = 32 * I_{adapter} * R_{sense}$$



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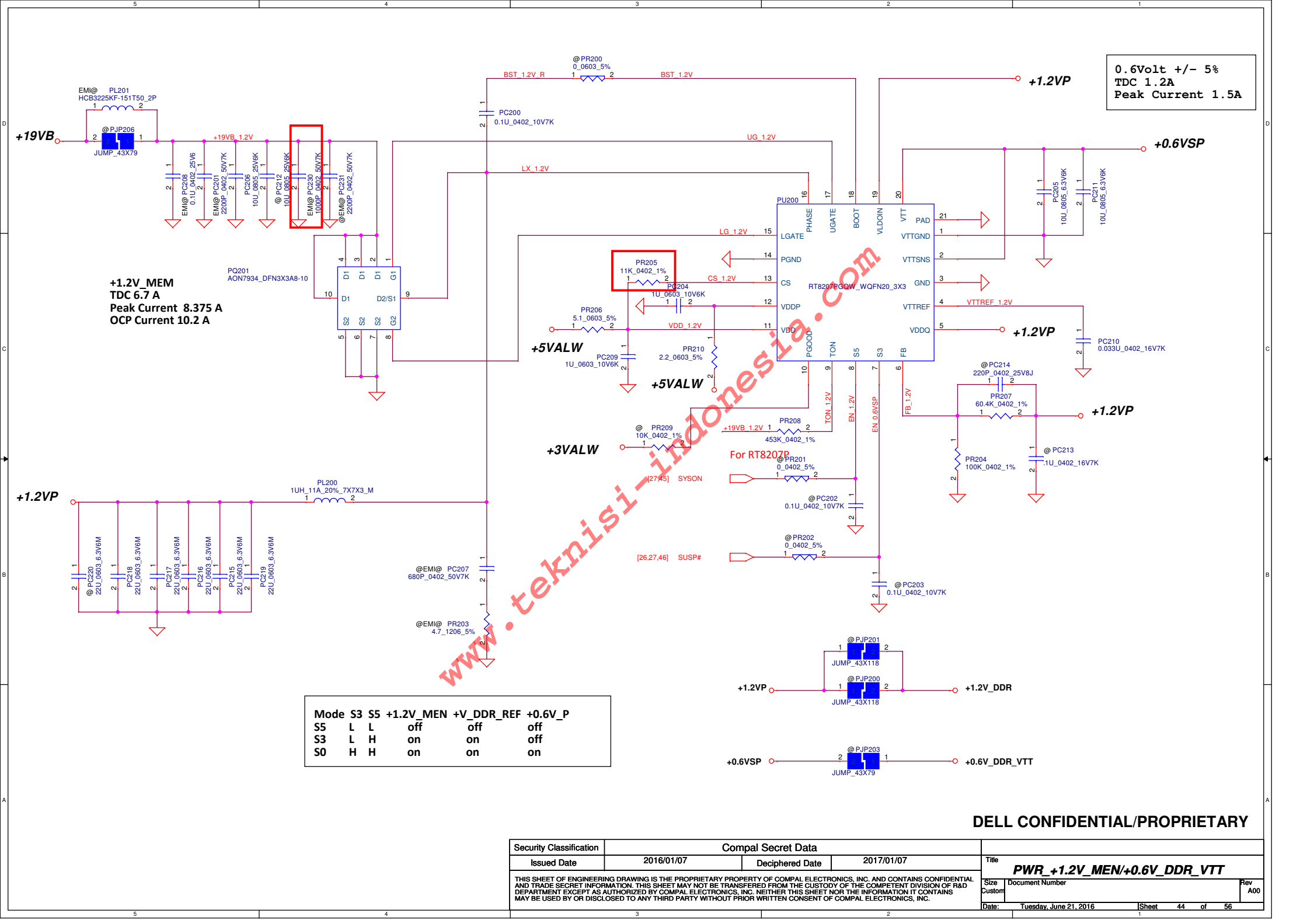
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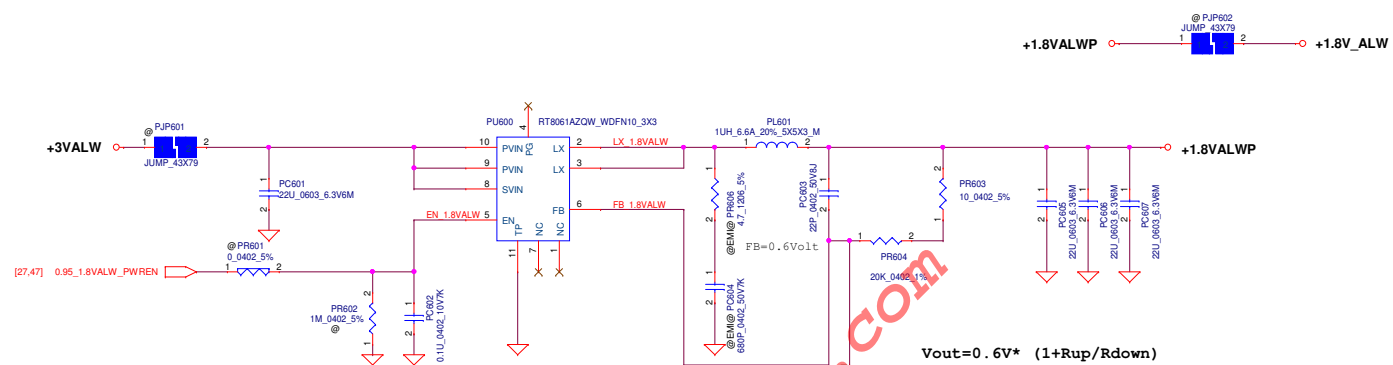


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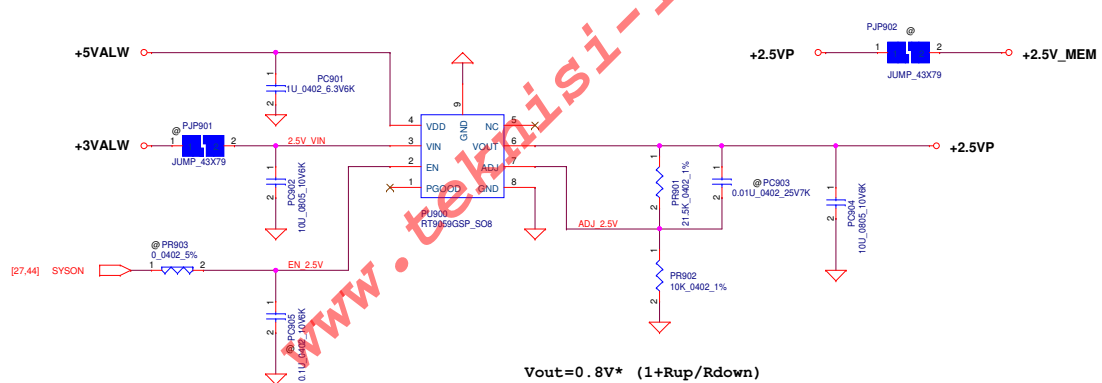
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| PWR_3.3VALWP/5VALWP | | | |
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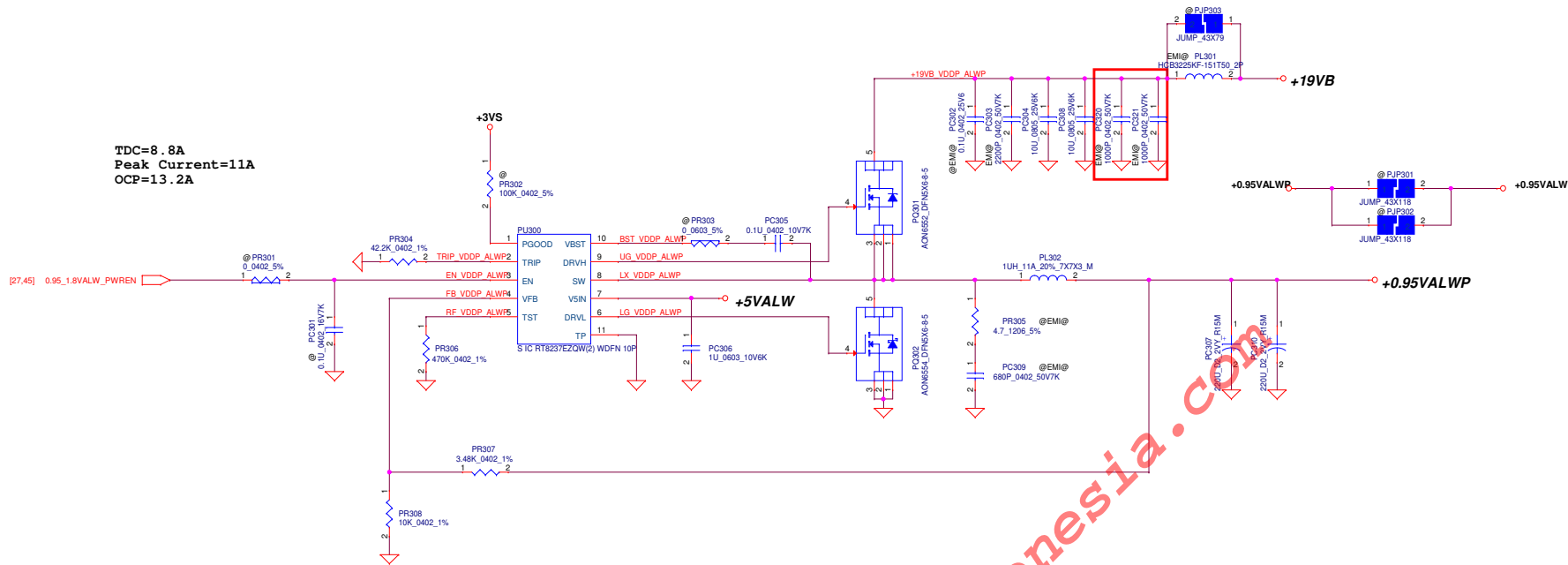
+1.8V PRIM
TDC 2 A
Peak Current 2.5 A
OCP Current 3.5A fix by IC



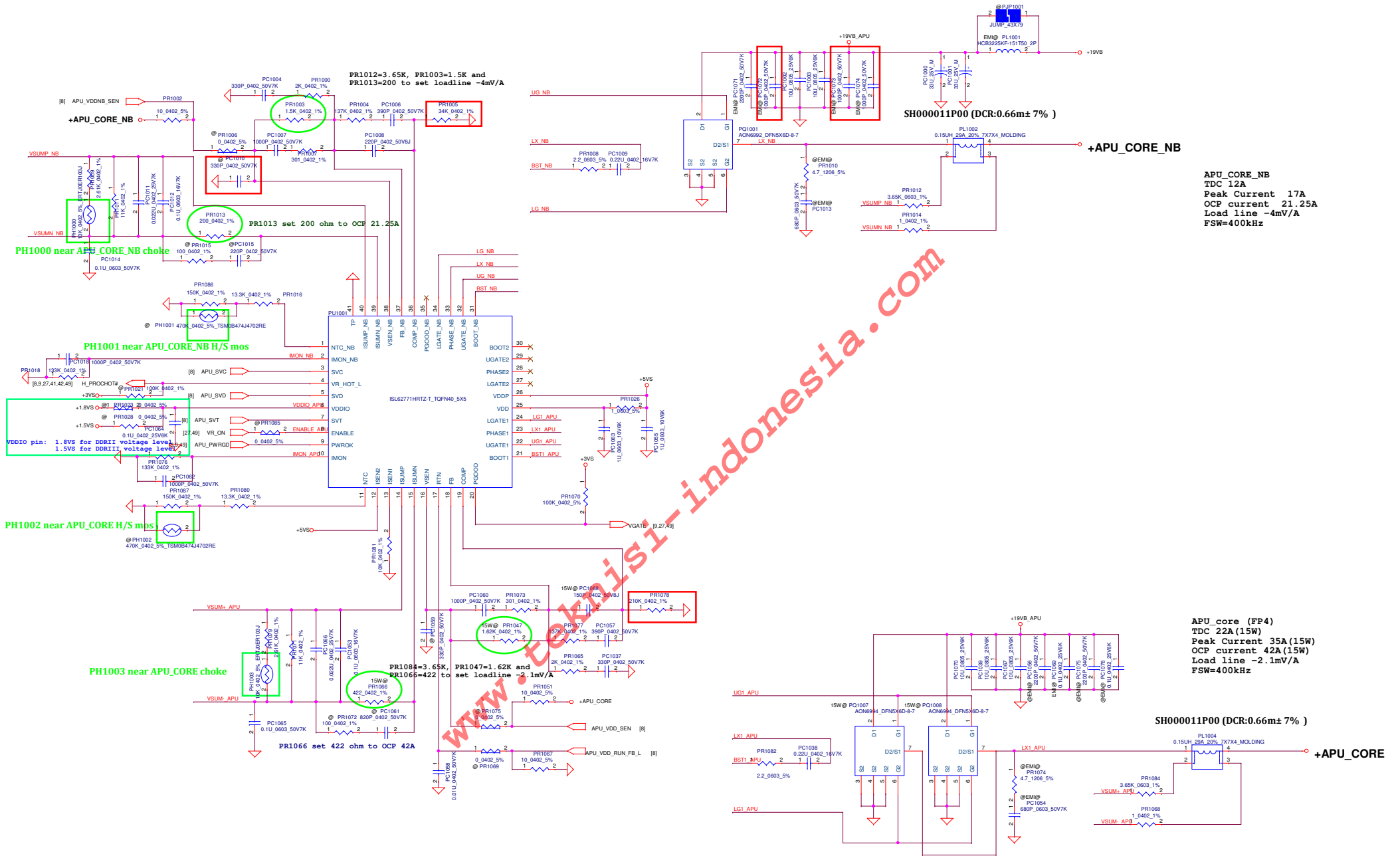
+2.5V
TDC 0.72 A
Peak Current 0.9 A

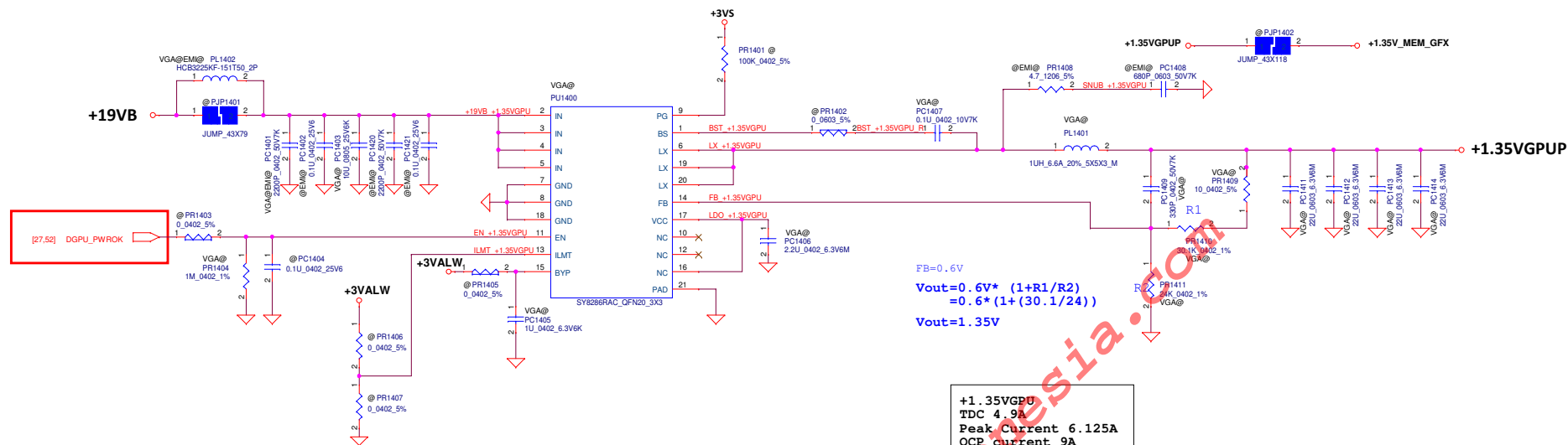
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| Date | Tuesday, June 21, 2016 | Sheet | 45 of 56 | A00 |

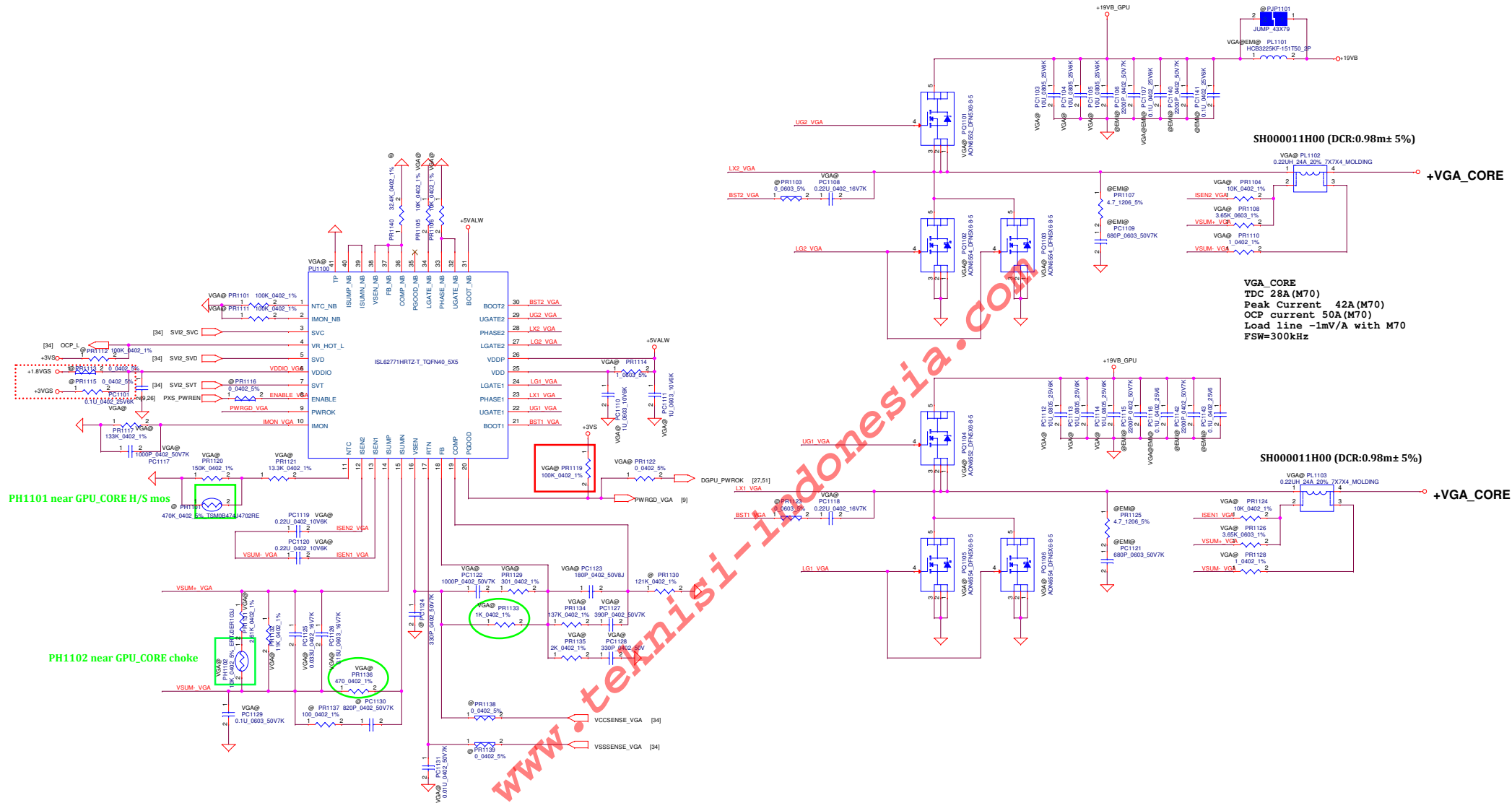


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| | | | | | Document Number |
| | | | | | Rev |
| | | | | | A00 |
| | | | | | Date: Tuesday, June 21, 2016 |
| | | | | | Sheet 47 of 56 |





| OCP setting | ILMT(pin13) |
|-------------|-------------|
| 6A | Pull low |
| 9A | Floating |
| 12A | Pull high |

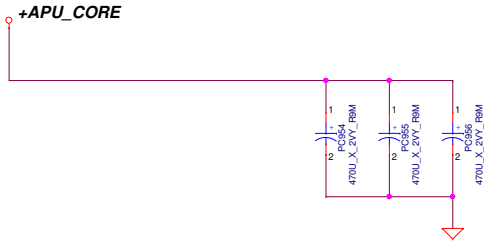


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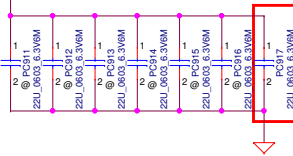
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| Security Classification | | Compal Secret Data | | Title | |
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+APU_CORE

APU_CORE
470uF*3

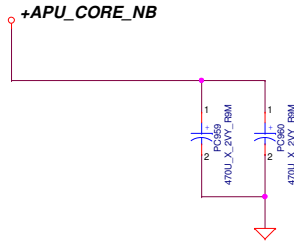


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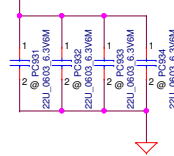


+APU_CORE_NB

APU_CORE_NB
470uF*2

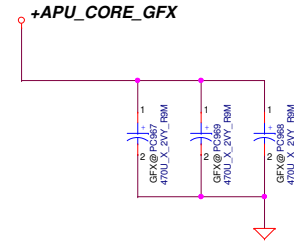


+APU_CORE_NB

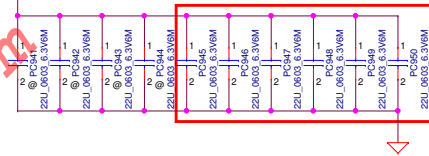


+VDDGFX

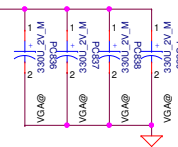
+VDDGFX
470uF*3



+APU_CORE_GFX



+VGA_CORE

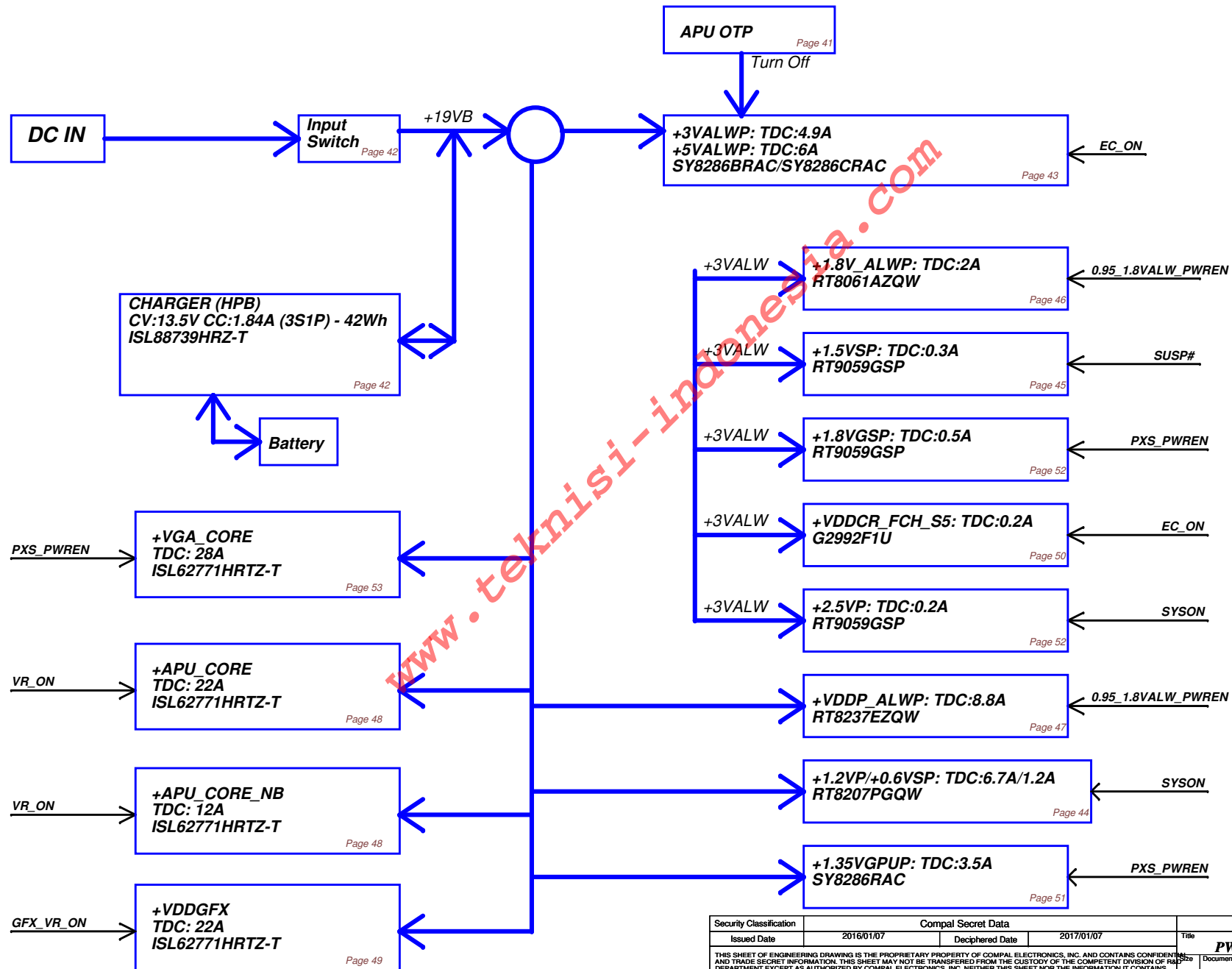


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| 2016/01/07 | | 2017/01/07 | | PWR PROCESSOR DECOUPLING | |
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Power block



Page 1

| | |
|---|--|
| change power limit from 11W to 17W by EE side | delete all P595 component |
| design change to adjust APU_CORE setting | delete PC1010 change PR1005 from 11.9K to 10.9K change PR1078 from 95.3K to 105.3K |
| design change to adjust GFX_CORE setting | add PR534 32.4K change PR520 from 95.3K to 105.3K |
| design change from EE recommend | add PR113 100K |
| adjust OTP setting from thermal recommend | change PR24 from 14K to 16.9K |
| design change to remove Erp lot6 circuit | delete PR2,PR5,PR7,PR10,PQ1 |
| adjust OCP setting | change PR205 from 8.25K to 10.25K |
| design change | change PQ740 from SB0000149 to SB0000150 |
| design change to meet stardust test result | add PC917,PC945,PC946,PC947 |
| design change from EMI recommend | change PC2,PC4 from 0.1u to 0.2u |
| design change | change PR103 from 499K to 1.0M |
| adjust OCP setting | change PR24 from 16.9K to 18.9K |
| | |

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| | | | | Document Number | Rev A00 |
| Date: | Tuesday, June 21, 2016 | Sheet | 55 | of | 56 |

DVT1 change list

| Item | Page | Date | Rev. | Reason for change | Modify Item |
|------|-------|------------|------|---|--|
| 1 | 26 | 2016/1/28 | 0.2 | modify the capacitor value | C621 change 1u_0603 capacitor to 4.7u_0603 |
| 2 | 26 | 2016/1/28 | 0.2 | modify the capacitor value | C620 change 4.7u_0603 capacitor to 1u_0603 |
| 3 | 26 | 2016/1/28 | 0.2 | Part count | C344 pop change to " DIS@ " |
| 4 | 13 | 2016/1/29 | 0.2 | Change Capacitor to H1.9 | CD229 Change to SGA20331E10 |
| 5 | 26 | 2016/3/13 | 0.2 | modify RC Delay for +1.8VGS | 1.8VGS_0.95VSDGPU_ON connect to U15.3 & U15.5 (R440 pop 47K, C624 pop 0.1uF) |
| 6 | 24 | 2016/3/13 | 0.2 | pop Q9 for touch-pad (PTP) | Q9 Change to pop |
| 7 | 16 | 2016/3/15 | 0.2 | Follow Intel KBL BOM to cost reduce | +LCDVDD power switch U1 change to SA000079400 |
| 8 | 11,18 | 2016/3/15 | 0.2 | Audio codec +1.5VS change to +1.8VS cost down +1.5VS LDO | Add RC18/RA15/RA16_reserve +1.5VS |
| 9 | 24 | 2016/3/15 | 0.2 | JKB1.30 remove KB_DET# (follow Tulip) | Add RE60 reserve to +5VS |
| 10 | | 2016/3/16 | 0.2 | part count reduce | change to R-short RC119, RA1,RA2,RA4,RA5,RL5,R16,RC53,RC52 |
| 11 | 10,25 | 2016/3/16 | 0.2 | change USB Port (AMD request) | USB20 Port7 change to Port2 (camera device) |
| 12 | 22 | 2016/3/16 | 0.2 | SATA net name modify | modify to SATA_TX_P0/N0 SATA_RX_P0/N0 |
| 13 | 22 | 2016/3/18 | 0.2 | remove SATA ESD, confirm with ESD team | Delete EU3101 |
| 14 | 17 | 2016/3/18 | 0.2 | for layout request swap RPI2 pin | Swap RPI2 pin |
| 15 | 9 | 2016/3/18 | 0.2 | BOM name error | R7C03 ---> RC703 |
| 16 | 9 | 2016/3/18 | 0.2 | modify VRAM config. | net name vram size/APU_ID/Panel size_ID change to VBIOS_ID1/D2/D3 |
| 17 | 6 | 2016/3/21 | 0.2 | add AMD FX-9800P CPU | Add FX-9800P CPU |
| 18 | 26 | 2016/3/21 | 0.2 | modify to meet the GPU power sequence | modify R438 1K ohm to 47K ohm |
| 19 | 30 | 2016/3/21 | 0.2 | ME drawing add a screw hole | add H13 H_6P0 screw hole |
| 20 | 24 | 2016/3/21 | 0.2 | Follow Intel KBL BOM to cost reduce | F3 SP040002400 change to SP040002B00 |
| 21 | 30 | 2016/3/21 | 0.2 | DFx review stand off pad can't place via | H11 H_3P2-G modify to H_3P2 |
| 22 | 18 | 2016/3/21 | 0.2 | vendor feedback have extra pull-up Resistor | remove RA46, RA47 |
| 23 | 29 | 2016/3/21 | 0.2 | remove PWR/Board unused pin | remove JPWR1.4 +5V/LW net name |
| 24 | | 2016/3/21 | 0.2 | fix Hi-Pot | LANGND Change to GND |
| 25 | 19 | 2016.01.14 | 0.2 | modify UL3 BOM config | remove UL3 BOM config |
| 26 | 26 | 2016.01.14 | 0.2 | modify R439 BOM config | add DIS@ BOM config to R439 |
| 27 | 34 | 2016.01.14 | 0.2 | modify RV164 BOM config | add DIS@ BOM config to RV164 |
| 28 | 18 | 2016.01.14 | 0.2 | modify CA42 BOM config | add 3234@ BOM config to CA42 |
| 29 | 26 | 2016.01.14 | 0.2 | modify GPU power sequence | C622, C623 change 4.7U 0603 to 0.1U 0402 and unpop |
| 30 | 9 | 2016.03.21 | 0.2 | unify name with stoney | AGPIO65 change to SKU_ID |
| 31 | 14 | 2016.01.14 | 0.2 | For cost reduce | unpop CD144 |
| 32 | 13 | 2016.01.14 | 0.2 | For cost reduce | change CD116 SGA00006A00 to SGA20331E10 |
| 33 | 16 | 2016.02.04 | 0.2 | Colay F1 | unpop R4 and pop F1 |
| 34 | 27 | 2016.01.14 | 0.2 | DVT1 board ID | RE22 0 ohm change to 12K ohm |
| 35 | 26 | 2016.02.04 | 0.2 | follow spec suggestion | C621 change 4.7U 0603 to 1U 0402 |
| 36 | 26 | 2016.02.04 | 0.2 | modify GPU power sequence | pop C344 |
| 37 | 18 | 2016.02.04 | 0.2 | Follow EMC suggestion | LA3, LA4, LA5, LA6 change SM01000E100 to SM01000NX00 (change part size 0603 to 0402) |
| 38 | 26 | 2016.02.04 | 0.2 | modify GPU power sequence | R438 change 1K ohm to 47K |
| 39 | 26 | 2016.02.04 | 0.2 | modify GPU power sequence | add C983 0.1uF |
| 40 | 27 | 2016.03.22 | 0.2 | EC require due to no use | unpop RE44,RE40,RE23,RE24,CE47 |
| 41 | 20 | 2016.03.22 | 0.2 | confirm EC use RW6,RW7 to debug | unpop RW9,RW10 |
| 42 | 26 | 2016.03.22 | 0.2 | Follow Intel KBL | add C625 0.1uF |
| 43 | 29 | 2016.03.22 | 0.2 | ME DFX require | JPWR1 change part |
| 44 | 22 | 2016.03.17 | 0.2 | meet DFX require | modify JHDD1 footprint |
| 45 | 13 | 2016.03.17 | 0.2 | For cost reduce | change CD117 SGA00006A00 to SGA20331E10 |
| 46 | 22 | 2016.03.17 | 0.2 | for fine tune sata redriver setting | unpop RS37,RS27,RS28,RS22 |
| 47 | 40 | 2016.03.17 | 0.2 | meet dell require | UV12,UV13,UV14,UV14 VRAM part change |
| 48 | 11 | 2016.03.24 | 0.2 | add+0.95 GFX power shape | delete LC22 |
| 49 | 8,27 | 2016.03.24 | 0.2 | add +APU_CORE power shape | delete APU_RST#_EC/APU_PWRGD_EC reserve compoent |

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DVT2 change list

| Item | Page | Date | Rev. | Reason for change | Modify Item |
|------|------|------------|------|-----------------------|---|
| 1 | | 2016.04.12 | 0.3 | reduce part count | change to R-short: RC20,RC1675,R12,R14,R7,R51,RA22,RA11,RA42,RE338,RE5,RE31,RE32,RE33,RE34,RE37,RE38,RE39,RE50,RE51,RE42 |
| 2 | 27 | 2016.04.13 | 0.3 | EC Board id change | RE22 12K 1% change to 15K 1% (SD034150280) |
| 3 | 16 | 2016.04.14 | 0.3 | reduce part count | change to R-short R6,R13,RX7 |
| 4 | 30 | 2016.04.21 | 0.3 | correct part | C35~C40 16V change to 25V rating (SE00000G880) |
| 5 | | 2016.04.21 | 0.3 | increase voltage rate | C4 10U 6.3V change to 10U 25V (SE00000X210) |
| 6 | | 2016.04.21 | 0.3 | increase voltage rate | C34,C2305,C2306,C2308,CA1,CA3,CU13,CU18 10U 6.3V change to 10U 10V(SE00000SU00) |
| 7 | | 2016.04.21 | 0.3 | increase voltage rate | CA11 4.7U 6.3V change to 4.7U 10V (SE00000MA00) |
| 8 | | 2016.04.21 | 0.3 | increase voltage rate | CF4 22U 6.3V change to 22U 10V (SE00000VJ80) |
| 9 | 29 | 2016.04.22 | 0.3 | follow ME require | change PWR CONN("E-T_6915K-Q06N-00L_6P") |
| 10 | 30 | 2016.04.23 | 0.3 | factory IQE require | modify H6 from 5 to 5.6 mm |
| 11 | 17 | 2016.04.29 | 0.3 | for layout modify | RP11 net swap |
| 12 | 17 | 2016.04.29 | 0.3 | for layout spacing | del CH11~CH18 emi part |
| 13 | 27 | 2016.05.03 | 0.3 | follow ESD require | CE23 change to pop |
| 14 | 21 | 2016.05.03 | 0.3 | follow EMI require | LA8,LA9(SD028000080) from bead change to 0 ohm 0402 |
| 15 | 30 | 2016.05.03 | 0.3 | follow EMI require | C35~C49 change to unpop |
| 16 | | 2016.05.03 | 0.3 | reduce part count | RC22,RC664,RA15,RC18,RD18,RD21,RA40,R37,RL9,RW11,RV164,RV27,RV30,RV364,RV31 |
| 17 | 29 | 2016.05.03 | 0.3 | follow ME require | Update JPWR1 footprint to "JXT_FP226H-006S1BM_6P" |

XB change list

| Item | Page | Date | Rev. | Reason for change | Modify Item |
|------|-------|------------|------|----------------------------------|---|
| 1 | 9 | 2016.05.21 | 1.0 | fixed PCIE wake on DC mode | reserve for RC667(0 ohm 0402) |
| 2 | 26 | 2016.05.31 | 1.0 | modify +0.95VGS/+1.8VGS sequence | C343,C344 From 550P to 1000P (SE074102K80) |
| 3 | 6 | 2016.06.03 | 1.0 | APU R3 PN | add APU R3 PN |
| 4 | 33 | 2016.06.03 | 1.0 | GPU M70 R3 PN | add GPU M70 R3 PN |
| 5 | 38,39 | 2016.06.06 | 1.0 | VRAM R3 PN | add VRAM R3 PN |
| 6 | 30 | 2016.06.06 | 1.0 | PCB R3 PN | add PCB R3 PN |
| 7 | 23 | 2016.06.06 | 1.0 | fixed factory usb 3.0 fail issue | change LU1,LU2,LU4,LU5 from SM070003V00 90 ohm to SM070004K00 67ohm |
| 8 | 9 | 2016.06.06 | 1.0 | fixed RTC idle 24hrs over +-2S | change CC682 from 22P to 18P |
| 9 | | 2016.06.06 | 1.0 | follow DFB suggestion | R17,R18,RU5,RU6,RU11,RU12,RU13,RU14,RU18,RU17,RU9,RU10,RI1,RI2,RI4,RI5,RI7,RI8,RI10,RI11,RU3,RU4,RU7,RU8,RU1,RU2 cover the solder mask ,so change footprint |
| 10 | 18 | 2016.06.06 | 1.0 | reduce part count | RA17,RA18,RA19,RA20,RA21 change to R_short |
| 11 | 27 | 2016.06.06 | 1.0 | EC board ID | RE22 from 15K(SD034150280) to 20K (SD034200280) |
| 12 | 24 | 2016.06.13 | 1.0 | follow DFB suggestion | JKB1 from SP01001LM00(S H-CONN ACES 50699-03041 30P) to SP01001LN00(S H-CONN STARCONN 132C30-100020 30P) |
| 13 | 29 | 2016.06.13 | 1.0 | reduce part count | reserve for SW1 SW2(For debug) on pilot run |

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| | | | | Rev | A00 |